How Do They Manage Designing Complex SOC?

Youn-Long Lin
National Tsing Hua University
Dept CS, NTHU
Hsin-Chu, Taiwan 300
+886-3-573-1072
ylin@cs.nthu.edu.tw

Advance in semiconductor manufacturing technology enables low-cost integration of huge number of heterogeneous components in a single chip for very complex applications such as cellular phone sets and digital still cameras. Unlike in the past when different types of IC designers only have to focus on their specific areas such as logic, memory, and analog, while the interface and integration task was left to the system designer at the board level. Now the difficult task has to been done before the chip is taped out. This effort usually involves multiple companies in different segment of industry chain and different countries. Only a concert effort by all parties involved is the success possible.

As more and more system companies are looking for SOC solutions to stay competitive while many IC design teams are transforming themselves into having SOC capability, it is beneficial to the VLSI design, automation and test community to share their experience with one another.

This special session consists of three 30-minute embedded tutorials. The purpose is to share with the audience the authors' experience in pulling together resources from multiple heterogeneous parties including industry and academics to design a state-of-the-art SOC for mass market digital still camera in the volume of millions of units. They are all related in the sense that university-developed technology has been transferred to the industry for practical use.

The first talk entitled "Integration, Verification and Layout of a Complex SOC" describes from an SOC design service provider's view how it supplies a digital still camera maker with a single chip controller. In addition to its IP portfolio, it has to collaborate with its wafer foundry partner and multiple third party IP vendors. The talk shows how they cope with unexpected difficulty during IP qualification, integrated verification, yield enhancement and failure analysis.

The second talk entitled "JPEG, MPEG4 & H.264 Codec IP Development" describes a university laboratory's effort in doing leading edge research in the field of VLSI architecture for image and video coding. It develops a JPEG encoding hardware accelerator that attracts industry attention. Collaboration with the industry proves helpful in later development of MPEG4 and H.264 Codec.

The third talk entitled "SOC Testing Methodology and Practice" describes the test design of a commercial digital still camera (DSC) controller chip, on which the author practice a novel SOC test integration platform, solving real problems in test scheduling, test IO reduction, timing of functional test, scan IO sharing, embedded memory built-in self-test (BIST), etc. Starting with SOC testing, the talk covers built-in self test (BIST) for embedded SRAM macros as well as SOC test integration tools and memory BIST compiler. Furthermore, testing of various IP cores in an SOC is developed and applied in production use.