Fall, 2023
Week 12
2023.11.27

組別：_____ **簽名：**_____

[group12]

1. Fill in the blanks according to the concept of pipeline.

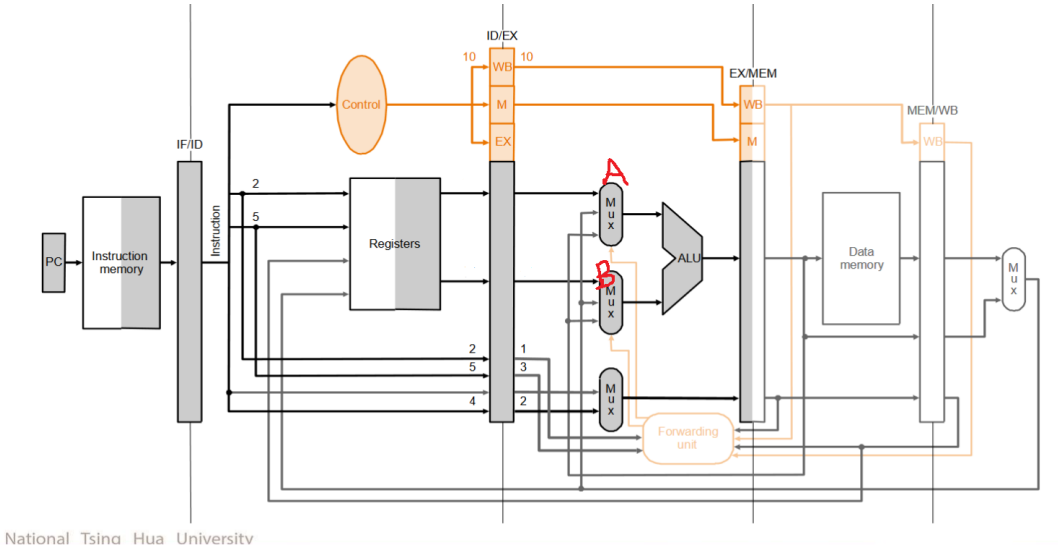
<table>
<tr><td colspan="6">Pipeline Hazards</td></tr>
<tr><td>structural hazards</td><td colspan="4">data hazards</td><td>control hazards</td></tr>
<tr><td rowspan="2">definition?</td><td colspan="2">RAW</td><td>WAR</td><td>WAW</td><td rowspan="2">definition?</td></tr>
<tr><td colspan="3">will occur in MIPS</td><td>won’t occur in MIPS</td></tr>
<tr><td rowspan="2">solution?</td><td colspan="2">solutions (for MIPS)</td><td colspan="2" rowspan="2">why?</td><td rowspan="2"></td></tr>
<tr><td>software
(1)</td><td>hardware
(1)
(2)</td></tr>
</table>

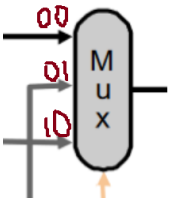
Ans :

<table>
<tr><td colspan="6">Pipeline Hazards</td></tr>
<tr><td>structural hazards</td><td colspan="3">data hazards</td><td colspan="2">control hazards</td></tr>
<tr><td rowspan="2">use the same resource in 2 different ways at the same time.</td><td colspan="2">RAW</td><td>WAR</td><td>WAW</td><td rowspan="2">definition?
attempt to make decisions before the condition is evaluated.</td></tr>
<tr><td colspan="2">will occur in MIPS</td><td colspan="2">won’t occur in MIPS</td></tr>
<tr><td rowspan="2">ensure all stages apply different resources</td><td colspan="2">solutions (for MIPS)</td><td colspan="2" rowspan="2">why?
all instructions take 5 stages, and reads are always in stage-2; writes are always in stage-5</td></tr>
<tr><td>software
(1)Inserting NOPs</td><td>hardware
(1)forward
(2)install</td></tr>
</table>

[group5]

2.





What are the values of MUX A and B in binary when we execute the instructions below? (Assume the instructions before them do not cause any hazards.)

1. sub $2, $1, $3
2. add $4, $2, $5
3. or $4, $4, $2
4. add $6, $2, $4

Instruction	MUX A	MUX B
sub $2, $1, $3		
add $4, $2, $5		
or $4, $4, $2		
add $6, $2, $4		

Ans:

Instruction	MUX A	MUX B
sub $2, $1, $3	00	00
add $4, $2, $5	10	00
or $4, $4, $2	10	01
add $6, $2, $4	00	10

[group4]

3.

True or False Question

a. In MIPs 5-stage pipeline, R-Type-use data hazard can be handled by Forwarding technique.

b. In MIPs 5-stage pipeline, forwarding technique is not enough to handle load-use data hazard since it takes longer to read memory than register.

c. The main reason why inserting NOP is not preferred is that software runs slower than hardware.

d. Using Forwarding technique, we always need to forward data if EX/MEM.RegisterRD == ID/EX.RegisterRS.

e. There is a register which will be written by instruction 1 and then read by instruction 2. Without forwarding, to avoid hazard, 3 stalls or NOPs will be inserted in instruction 2 to make sure that the instruction 2 will read the right data from the pipeline register.

f. The main difference between inserting NOP and Stalls is that the previous one is detected by the compiler and the latter one is detected by hardware.

Ans:

TFFFFT

a. T

b. F, since memory-read ends after the next instruction using ALU.

c. F, only inserting NOP will waste many cycle times.

d. F, not necessary if EX/MEM.RegisterRD == $0.

e. F, 2 stalls or NOPS will be used.

f. T

[group3]

4. Considering the forwarding unit in a 5-stage pipelined processor, please answer T/F for each statement.

   (1) The forwarding unit is a kind of sequential circuit.

   (2) The forwarding unit detects the true data dependency for EX pipeline stage and selects the forwarded results for the execution unit.

   (3) The forwarding unit is a pipeline register.

   (4) The forwarding unit compares the source register number of the instructions in the MEM and WB stages with the destination register number of the instruction in the decode stage.

   Ans:

   (1) False. Sequential circuits are digital circuits that store and use the previous state information to determine their next state. However, the forwarding unit only consider the current inputs.

   (2) True

   (3) False

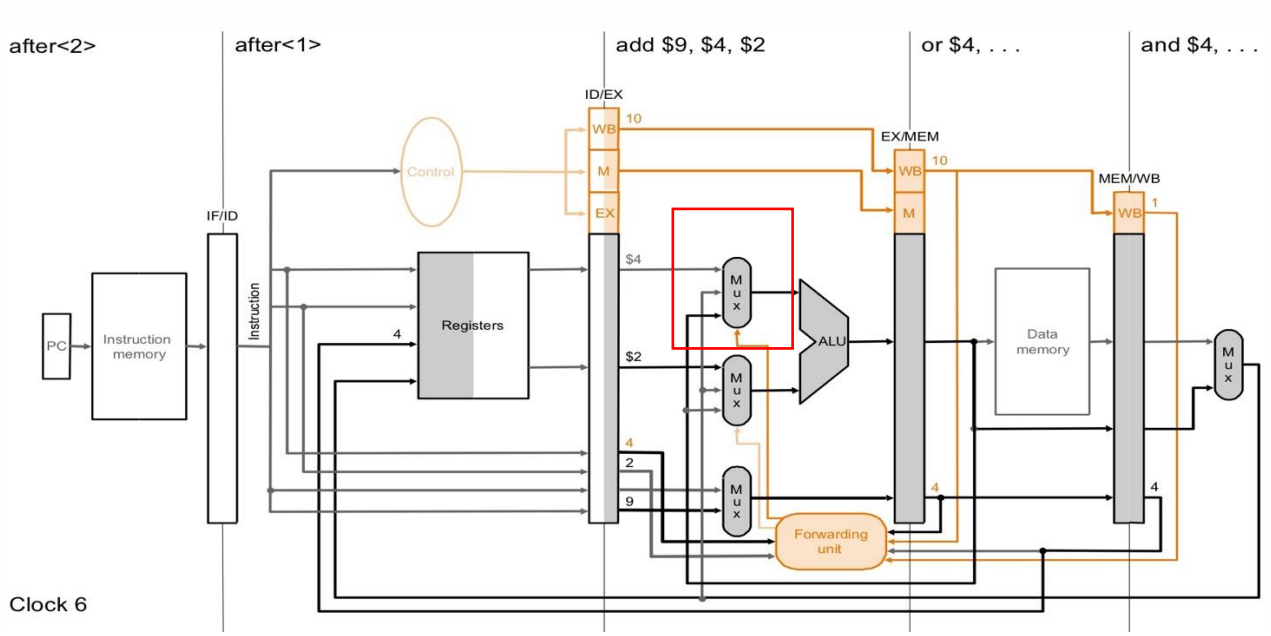
   (4) False. The forwarding unit compares the destination register number of the instructions in the MEM and WB stages with the source register number of the instruction in the decode EX stage.

[group6]

5. Choose the correct statements.

(A) Forwarding is necessary if we encounter data hazard conditions.

(B) According to the below picture, the control signal for Mux 1 should be 01



(C) Based on the following condition

if (ID/EX.MemRead) and (ID/EX.RegisterRt = IF/ID.RegisterRs)

it is a detection for stalling

(D) Using internal forwarding can solve the problem when two instructions (one in WB stage and the other in ID stage) are running in the same cycle

Ans: (C)(D)

(A) F, don't need if the instruction does not write register or if the destination register is $0

(B) F, 10

(C) T

(D) T

[group7]

6. Which of the following statements are true for the forwarding unit in a 5-stage pipelined register?

(1) The forwarding unit is used to bypass the write-back result due to structure hazard.

(2) The forwarding unit forwards an execution result before it is written back to a destination register.

(3) The load-use data hazard can solve by forwarding without other technique.

(4) The forwarding unit compare the destination register number of the instruction in the MEM and WB stages with the source register number of the instruction in the EX stage.

(5) If the same register in WB and MEM need to forward to the ALU, we should select the input from the MEM stage.

Ans:

(2), (4), (5)

1.the forwarding unit is used to bypass the write-back result due to data hazard.

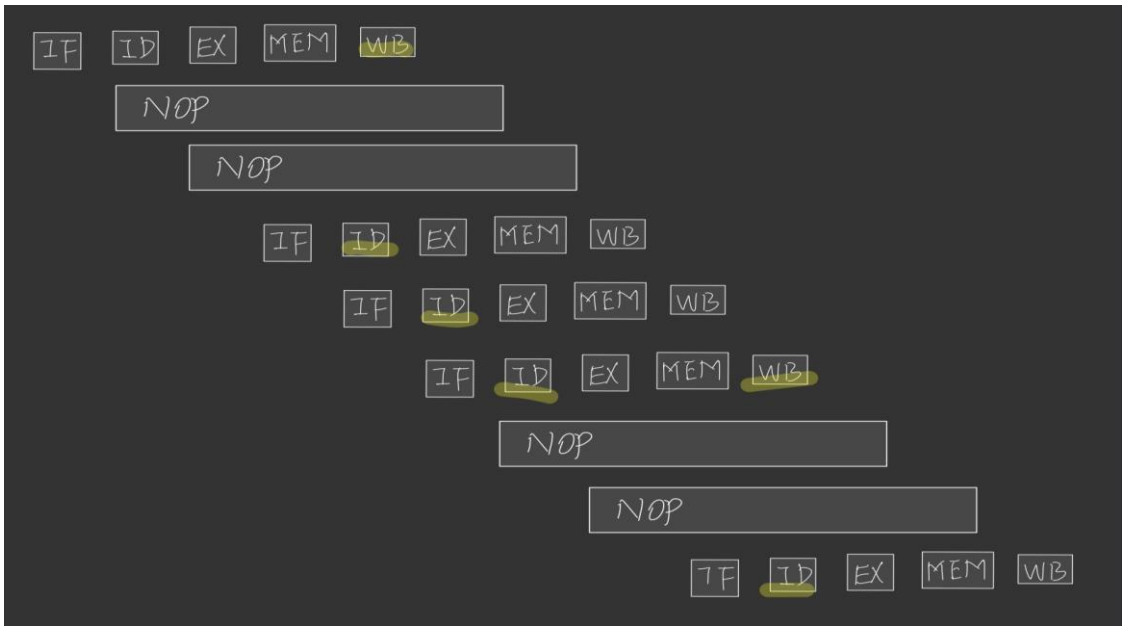
3.the load-use data hazard can solve by stall and forward.

[group8]

7. Please give a brief description of data hazards and indicate where should insert the NOPs to resolve the below program. Also indicate how many NOPs you use.

   sub $2, $1, $3
   and $7, $2, $5
   or $8, $6, $2
   add $2, $9, $2
   sw $10, 20($2)

Ans: Data hazards: Attempt to use items before ready.



[group9]

8. True or False regarding pipeline hazard:

(a) An example of structural hazards can be the condition when two instructions are accessing the same memory in the same cycle.

(b) “Forwarding” is a common technique to relieve the control hazards.

(c) Control hazard arises from the need to make a decision based on the result of one instruction (e.g. branch instruction) while others are executing.

(d) Structural hazard arises from the dependency of one instruction on an earlier one that is still in the pipeline.

(e) Generally speaking, a pipeline hazard happens when the next instruction cannot execute correctly in the following clock cycle.

Ans:

(a) T

(b) F. Data hazard

(c) T

(d) F. Data hazard

(e) T