Advanced Logic Synthesis (CS613200) - Final Project

Instructor: Prof. TingTing Hwang

Due date: 2025/06/13 (Fri.)

1. Project Description

This project focuses on logic synthesis for FPGA mapping. Given a Boolean circuit described in BLIF format, your goal is to perform logic decomposition and K-input LUT mapping to optimize for delay (circuit level) and area (number of LUTs).

Input/Output Format

- **Input file:** A BLIF file containing Boolean logic (AND, OR, NOT, CONST).
- **Output file:** A BLIF file representing the mapped circuit using K-input LUTs.
- **Standard output:** Must include:
  - The circuit level.
  - The number of LUTs.

Execution Example:

```
%> ./map -k 4 map01.blif output.blif
The circuit level is 2.
The number of LUTs is 5.
```

2. Notice

1. The score is based on the product $level \times |LUTs|$. For detailed evaluation, refer to the provided README file.
2. You must **implement your own technology mapping code**. Calling any external mapping tools (e.g., ABC, Yosys, etc.) for this purpose is strictly prohibited.
3. You **may use external tools (such as ABC or SIS)** for circuit preprocessing (e.g., strashing, optimization), but not for mapping.
4. The specific mapping algorithm is not restricted.
5. The output circuit must be functionally equivalent to the input circuit. Use the ABC command `cec` to verify correctness.
6. TA will test your implementation with various k values for the LUT.
7. Each test case must finish within **1 minute**. The size of hidden test circuits is similar to that of the public test cases.
8. A written report is **not mandatory**, but providing one will be appreciated.

9. During the demo, you must clearly explain your **data structures**, **algorithms**, and **experimental results**. TA may inspect portions of your code to ensure it is your own work.

10. During the demo session, the TA will upload your code to the CAD Server, compile it on-site, and run test cases to grade your submission.

11. Please refer to the provided `final_project.tar.gz` archive for more details and grading criteria.

3. References

- J. Cong, Y. Ding, "An Optimal Technology Mapping Algorithm for Delay Optimization in Lookup-Table based FPGA Designs," *IEEE TCAD*, Vol. 13, No. 1, Jan. 1994, pp. 1–12.

- Berkeley Logic Interchange Format (BLIF), UC Berkeley.
Available at: https://course.ece.cmu.edu/ ee760/760docs/blif.pdf

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