**2002 IC/CAD Contest**
**Problem 5: Two-level Boolean Minimization**
**Source: Springsoft Inc.**
**Dec 31 2002**

## I. Introduction and Problem Definition

Two-level Boolean minimization attempts to minimize the sum-of-product (SOP) representation of a multiple output Boolean function so that the number of product terms and the number of literals for the function is reduced. Previously, there are two approaches for solving two-level minimization - *exact* and *heuristic* methods [4,5,6,7]. In general, the exact algorithms take two steps in finding a minimum cover:

1. Generation of the set of all **prime product-terms** for a given function.
2. **Selection** of a minimum set of prime terms to implement this function

Usually an exact algorithm (such as Quine-McCluskey method [2]) can find an optimum solution but may take large computing time for large circuits (with inputs number > 16) since it needs to generate all prime terms first. On the other hand, a heurist algorithm like Espresso [1] iteratively applies greedy approaches to improve a given initial SOP form until no improvement can be made. Usually, heuristic methods only obtain a local optimum solution rather than a global optimum one but they can be applied to large circuits.

## II. Input/Output Specification

The default input and output file formats should be compatible with the Berkeley standard format of a PLA [3]. The input format is described in detail in appendix A. Attendees need to implement a PLA reader for this format and also output the minimized Boolean function in the same PLA format. An example of input/output PLA format for a Boolean function can be found in Appendix B.

## III. Language/Platform

1. Language: C or C++.
2. Platform: SUN OS/Solaris, IBM PC.

## IV. Evaluation

The score will be given based on correctness, time efficiency and memory requirement.

## V. Questions

Please report any question regarding to this problem to cad@cs.nthu.edu.tw with the email subject “CAD Contest: Problem 5” Your question(s) will be answered in two weeks, and the Q&A’s will be posted at the contest Web site.

## VI. Reference


**[1]** Espresso:
http://www-cad.eecs.berkeley.edu/Software/software.html

**[2]** Quine-McClusky Minimization Method:
http://www.cs.byu.edu/courses/cs143/reading/quine.html

**[3]** PLA format:
http://www.engineering.uiowa.edu/~switchin/espresso.5.html

**[4]** "Synthesis and Optimization of Digital Circuits", Giovanni De Micheli, McGraw Hill Inc., 1994.

**[5]** "Logic Synthesis", Srinivas Devadas, Abhijit Ghosh and Kurt Keutzer, McGraw-Hill Inc., 1994.

**[6]** "Logic Synthesis and Verification Algorithms", Gary D. Hachtel and Fabio Somenzi, Kluwer Academic Publisher, 1996.

**[7]** “ESPRESSO-SIGNATURE: A New Exact Minimizer for Logic Functions “Patrick C. McGeer , Jagesh V. Sanghavi ,Robert K. Brayton , Alberto L. Sangiovanni-vincentelli ,DAC,1996


## Appendix A

A simple example of PLA format looks like:

```
.i 4
.o 3
0000  000
0001  001
0010  01-
0011  011
01-0  001
0101  0-0
```

*0110 011*
*01-1 100*

where the
.i [d] means the number of input variables

.o [d] means the number of output functions

Input plane:

Each position in the input plane corresponds to an input variable where a 0 implies the corresponding input literal appears complemented in the product term, a 1 implies the input literal appears uncomplemented in the product term, and – implies the input literal does not appear in the product term.

Output plane:

For each output, a 1 means this product term belongs to ON-set, a 0 means this product term has no meaning for the value of this function, a – means this product term belongs to DC-set.

**Appendix B**

Given a single output Boolean function f(w,x,y,z) with four inputs and its K-map shown below:

| wx \ yz | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | | 1 | 1 |
| 01 | 1 | | X | 1 |
| 11 | | 1 | X | |
| 10 | | 1 | 1 | |

In the above K-map representation, a 1 means this minterm belongs to the ON-set of function f, and a X means it belongs to the DC-set of f. The remaining minterms belong to the OFF-set. An example of input PLA format for Boolean function f is shown below:

**INPUT Format**

*.i 4*

*.o 1*
*0-00 1*
*001- 1*
*0110 1*
*1-01 1*
*-011 1*
*-111 -*

After a two-level minimization, the output PLA format might be as shown below:

**Output Format**

*.i 4*
*.o 1*
*0--0 1*
*--11 1*
*1--1 1*