2002 IC/CAD Contest

Problem 3: Scan Chain Reorder

Source: Faraday.

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I. Introduction

Recently, the power issue on the DFT field catches many people's eye. As we know, an ATPG pattern will try to exercise as much part of the design as possible. The power consumption during testing will be much higher than the normal operation. One of the most concerned issues is that the large peak power may cause the functional fail during testing, i.e., a good chip may not pass the ATPG pattern due to the excessive peak power consumption. To reduce the peak power consumption during testing, several works can be done at different aspects. One of these is to re-order the scan cells in the scan chain to reduce the peak power consumption during the scan chain shift stage. For example, assume the pattern to be shifted into an 8-bit scan chain is 01010101, all DFFs in this scan chain will transit simultaneously at the last cycle of the shift procedure. However, if the scan-chain is reordered to make the pattern become 11110000, it is clear that only one DFF will transit at each cycle during the whole shift procedure, as shown in Figure 1. In this figure, the arrow above a DFF indicates the direction of the transition in the DFF.

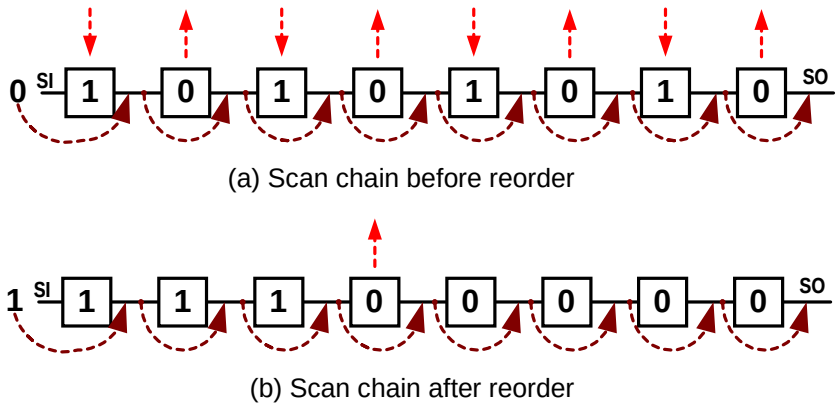

Figure 1 The last cycle of the scan chain shift procedure.

The objective of this problem concerns about the re-order of scan cells in the scan chain so that the given constraints are met and the peak power is minimized. The constraints include a)

Maximum peak power consumption b) Maximum scan chain length c) Maximum distance between two successive DFFs.

To judge whether the result of the re-ordered scan chain is good or not, three indexes will be taken into consideration, including maximum peak power consumption, scan chain length and execution time. In addition, different problem may have different weight on these three indexes, and the weight number will be written in the constraint file.

In order to simplify the problem, we make the following assumptions. (1) All scan cells have been reset to 0 before applying the first scan pattern. (2) A new pattern can be shifted into the scan chain only if the previous one has been shifted out. Under these assumptions, only the bit transitions **inside** the scan patterns have to be considered in the peak power calculation.

II. Maximum Peak Power Calculation

To simply the problem, it is assumed that a DFF will only consume power during logic transitions, and the peak power consumption is a given fixed value that is independent of the states of other DFFs. Each DFF will be given a specific value, which is determined by the capacitive load of the fan-out circuitry driven by the DFF.

It is also assumed that the peak power of all DFFs will occurs at the same time in the same cycle, i.e., no timing issue needs to be taken into consideration. The peak power consumption of the scan chain in a specific cycle could be easily calculated by the summation of the peak power consumption of all the DFFs that transited in this cycle.

For example, if 4 DFFs transited in one cycle and the peak power values for these 4 DFFs were given as [3.5, 5.7, 3.8, 1.3], the peak power of this cycle can be calculated as 3.5+5.7+3.8+1.3=14.3.

The maximum peak power for a specific scan chain under a given pattern is calculated by the selection the maximum peak power during the whole shift cycles.

For example, an 8-bit scan-chain will need 8 cycles to shift in a scan pattern and the peak power for these 8 cycles are [14.3, 9.4, 24.6, 11.9, 8.3, 25.6, 7.8, 9.5]. The maximum peak power for this scan chain pattern is 25.6.

The maximum peak power for the whole scan procedure is calculated by the selection of the maximum peak power among all the scan chain patterns.

III. Scan Chain Length Calculation

To represent the physical location of DFF in the layout, each DFF will be assign a coordinate with x and y. Assume there are two DFFs with coordinates (x1, y1) and (x2, y2), respectively. The distance between these two DFFs is calculated by $|x1-x2|+|y1-y2|$.

The length of the whole scan chain should be calculated by the accumulation of all the distances between successive DFFs in the scan chain.

IV. Input Data

1. Scan chain declaration file: this file is used the store the scan chain information. The format is as the following:

```
Cell1<x1,x2> 3.75
Cell2<x2,y2> 6.32
Cell3<x3,y3> 2.41
…
```

Figure 2 Scan Chain Declaration File Example

Each line in this file represents a scan cell and the line order represent the scan chain order. The first line represents the scan cell connecting the scan input pin and the last line represents the cell connecting to the scan output pin.

In each line, the two tupple <x,y> represents the coordinate of the scan cell and the last value represents the peak power consumption for the scan cell during logic transition.

2. Scan Pattern File: this file will store the pattern to be shift into the scan chain. The format is as the following:

```
010011001
110110110
001100101
…
```

Figure 3 Scan Chain Pattern Example File

Each line in this file represents a pattern to be shifted into the scan chain. The LSB is the value to be shifted into the scan cell connected to the scan input, and the MSB is the value to be shifted into the scan cell connected to the scan output. In other words, the MSB is to be shifted first while the LSB is to be shifted last.

3. Constraint file: this file contains the user specified constraints. The format is as following:

```
MaxPeakPower 300
MaxScanChainLength 150
MaxDFFsDistance 20
PeakPowerWeight 70%
ScanChainLengthWeight 10%
```

```
ExectionTimeWeight 20%
```

Figure 4 Example Constraint File

The first three lines represent the re-ordering constraints and the other lines represent the weight values for the three judge indexes. The grading of each index will be described later.

V. Output Data

1. A scan chain declaration file should be generated according to the re-ordered scan chain. The format must be the same as the input scan chain declaration file.
2. A re-ordered scan chain pattern should be generated. The format must be the same as the input scan chain pattern.
3. A report file should be generated according the following format:

```
Original Data:
    ScanChain Length = 130
    MaxPeakPower = 37.2

Reordered Data:
    ScanChain Length = 100
    MaxPeakPower = 24

Execution Time: 130.2 s
```

Figure 5 Example Report File

VI. Grading Strategy for the Program Efficiency

- 5 test case will be used to judge the efficiency of the scan re-order program, and each will be assigned 20% of the final score.
- The total score for a test case is 100.
- If core dump occurs or the execution-time is more than 8-hours for a test case, the score for this test case will be 0.
- If a solution does exist for a test case but the execution result doesn’t meet the constraints, the score for this test case will be 0.
- If the execution result meets all the constraints for a test case, the score for this test case will be started from 60.
- As mentioned before, three indexes (i.e., Maximum peak power, scan chain length and execution time) will be used to judge the efficiency of the scan re-order program. The score calculation for each index is as following:

1. All the execution results for a judge index for a test case generated from the attendees' programs will be collected first.
2. The execution result will be normalized from 0 – 40 and the value is the score for this judge index on this test case for the attendee's program.

- Total degree for a test case is calculated as follow:
  PeakPowerWeight*PeakPowerScore+ ScanChainWeight* ScanChainScore + ExecutionTimeWeight * ExecutionTimeScore + 60.

VII. Questions

Please report any question regarding to this problem to cad@cs.nthu.edu.tw with the email subject "CAD Contest: Problem 3." Your question(s) will be answered in two weeks, and the Q&A's will be posted at the contest Web site.