CS 4120 – Hardware Description Languages and Synthesis

Class Time: T5T6R8

Location: EECS 132

Instructor: 王廷基 EECS 643
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Office Hours: T7T8R7 or by appointment

TA: 萧威志 EECS 221
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Prerequisites: CS 2102 Logic Design or equivalent


Objectives: You will learn to design and simulate digital systems with Verilog HDL, and to use commercial CAD tools for automatic synthesis.

Web site: www.cs.nthu.edu.tw/~tcwang/cs4120.html

Grading Policy: Homework: 40%
Exam 1: 30% (in class, Tuesday, April 15, 2003)
Exam 2: 30% (in class, Tuesday, June 10, 2003)