Computer Architecture

Fall, 2026
Week 10
2026.11.9

組別：_____ **簽名：**_____

[group 8]

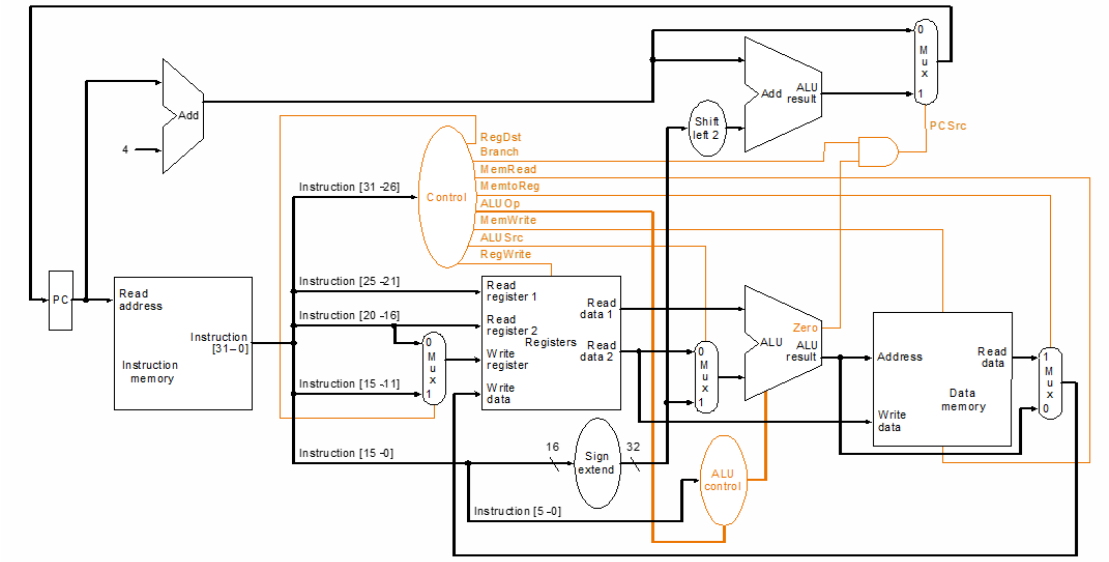
1. For a lw instruction, what ALUOp does the main control unit send, and what operation does the ALU perform?

Ans:

ALUOp = 00, and the ALU performs add (base register + offset) to compute the memory address.

[group 11]

2. The MIPS single-cycle processor has 9 bits main control signals. What are the values of these signals for the add, lw, and beq instructions?



Ans:

Control Signal	add (R-type)	lw (Load Word)	beq (Branch Equal)
RegDst	1	0	0
ALUSrc	0	1	1
MemtoReg	0	1	X
RegWrite	1	1	0
MemRead	0	1	0

MemWrite	0	0	0
Branch	0	0	1
ALUOp1	1	0	0
ALUOp0	0	0	1

[group 2]

3. A single-cycle MIPS CPU has these delays: PC clock-to-Q 30 ps, instruction memory 200 ps, register file read 100 ps, ALU 150 ps, data memory 200 ps, register file setup 20 ps, and clock skew 10 ps. Which instruction will be the critical path? What is the minimum clock period?

Ans: The critical path is the lw instruction, which uses every major block: 30 + 200 + 100 + 150 + 200 + 20 + 10 = 710 ps.

[group 7]

4. A single-cycle MIPS processor uses a 6-bit opcode, op5 op4 op3 op2 op1 op0 to identify the instruction type. The opcodes of five supported instruction types are shown below.

R-type opcode: 000000

lw opcode: 100011

sw opcode: 101011

beq opcode: 000100

jump opcode: 000010

(1) Determine the value of RegWrite for each instruction type

(2) Write the Boolean expression for RegWrite in terms of the opcode bits op5 through op0, and explain why.

Ans:

(1)

R-type: RegWrite=1

lw: RegWrite=1

sw: RegWrite=0

beq: RegWrite=0

jump: RegWrite=0

(2)

R-type = op5’ ·op4’ ·op3’ ·op2’ ·op1’ ·op0’

lw=op5·op4’ ·op3’ ·op2’ ·op1·op0

Therefore, RegWrite

= R-type + lw

= op5’ ·op4’ ·op3’ ·op2’ ·op1’ ·op0’ + op5·op4’ ·op3’ ·op2’ ·op1·op0

[group 1]

5. Describe the five stages of the MIPS pipeline and explain what happens in each stage.

Ans:
IF (Instruction Fetch): Fetches the instruction from instruction memory.
ID (Instruction Decode): Decodes the instruction and reads registers.
EX (Execute): Performs ALU operations or calculates memory addresses.
MEM (Memory Access): Reads from or writes to data memory.
WB (Write Back): Writes the result back to the register file.

[group 14]

6. What is the minimum number of cycles needed to completely execute n instructions on a CPU with a k stage pipeline? Justify your formula.

Ans:

$n + k - 1$.

Let's look at when each instruction is in the WB stage. In a k-stage pipeline, the 1st instruction doesn't enter the WB stage until cycle k. From that point on, at most one of the remaining $n-1$ instructions is in the WB stage during every cycle.

This gives us a minimum of $k + (n-1) = n + k - 1$ cycles.

[group 6]

7. 從 Clock Cycle 的角度，比較 Single-Cycle Processor 和 Pipelined Processor 的差異。

Ans:

Single-Cycle:每個 clock cycle 完成一條 instruction，有較長的 clock period

Pipeline:每個 clock cycle 完成一個指令的階段，有較短的 clock period，可以並行處理提高 throughput

[group 13]

8. Answer the following question:
   (1) What are the five stages of the MIPS pipeline?
   (2) In which stage are registers read/written?
   (3) In which stage does the ALU operate?

Ans: (1) IF / ID / EX / MEM / WB

(2) ID / WB

(3) EX

[group 10]

9. 某 MIPS Processor 採 IF、ID、EX、MEM、WB 五階段 Pipeline。假設 Single-Cycle 的 Clock Period 為 800 ps，Pipelined 的 Clock Period 為 200 ps；無額外的 Hazard、Stall 或 Pipeline Register 延遲。依序執行以下五條彼此沒有資料相依的指令：

```
I1: lw   $t0, 0($s0)
I2: sub $t1, $s1, $s2
I3: and $t2, $s3, $s4
I4: sw   $s5, 4($s6)
I5: or   $t3, $s7, $a0
```

(a) 畫出五條指令的 Pipeline Timing Table，指出執行完全部指令所需的 Clock Cycles。

(b) 分別計算 Single-Cycle 與 Pipeline 的總執行時間，以及 Pipeline Speedup。

(c) 以 lw 為例，將 ID 階段產生的控制訊號分為 EX、MEM、WB 三組，說明其內容和傳遞方式。

Ans:

(a) Pipeline Timing Table（— 表示該 Cycle 不在 Pipeline 中；MEM* / WB* 為不執行實質存取或寫回的階段）：

指令	C1	C2	C3	C4	C5	C6	C7	C8	C9
I1: lw	IF	ID	EX	MEM	WB	—	—	—	—
I2: sub	—	IF	ID	EX	MEM*	WB	—	—	—
I3: and	—	—	IF	ID	EX	MEM*	WB	—	—
I4: sw	—	—	—	IF	ID	EX	MEM	WB*	—
I5: or	—	—	—	—	IF	ID	EX	MEM*	WB

五階段、五條指令且沒有 Stall，所需 Cycles = 5 + 5 − 1 = 9 cycles。

(b) Single-Cycle Time = 5 × 800 = 4000 ps。

Pipeline Time = 9 × 200 = 1800 ps。

Speedup = 4000 / 1800 ≈ 2.22 倍。

速度提升未達 800 / 200 = 4 倍，因為有限條數的指令需要填滿與排空 Pipeline。

(c) lw 的控制訊號分組如下：

階段	控制訊號	用途
EX	RegDst = 0；ALUOp = 00；ALUSrc = 1	選 rt 為目的暫存器，ALU 執行位址加法
MEM	Branch = 0；MemRead = 1；MemWrite = 0	從 Data Memory 讀取資料
WB	RegWrite = 1；MemtoReg = 1	將讀出的記憶體資料寫回 rt

控制訊號在 ID 產生；隨資料先存入 ID/EX，之後必要的 MEM、WB 控制訊號依序傳至 EX/MEM、MEM/WB，在對應階段生效。

[group 12]

10. 假設執行：lw $t0, 0($s0)

當這條 lw 正在 EX Stage 時：

請回答兩個問題：

ALUSrc 應該是 0 還是 1？

RegWrite 此時應該已經對 Register File 生效了嗎？為什麼？

Ans:
1. ALUSrc = 1

因為：

在 EX 階段要計算：

ALU 的第二個輸入必須選擇 Sign-extended Immediate，所以 ALUSrc = 1。

2. RegWrite 還沒生效

lw 在 EX 階段只是計算地址。

它還要經過：

MEM：從 Data Memory 讀取資料。

WB：使用 RegWrite=1，把資料寫回 $t0。

[group 4]

11. Give a 5-stage pipeline processer.
    (a) At which stage is the control signal generated?
    (b) What would happen if you forgot to add registers to the control signals?
    (c) Why do the registers in each stage have different widths?

Ans:
(a) It is generated at stage instruction decode.
(b) An instruction requiring an ALU addition (e.g., add) might instead trigger a memory write or branch condition if the subsequent instruction in ID is a sw or beq. And it might write corrupted to incorrect location for a RegWrite or MemWrite instruction.
(c) For example, control signals like ALUOp, ALUSrc are consumed at the execution stage so they do not need to be passed forward to further stages. And the IF/ID stage have only 64 bit width because it only saves instructions and the PC.