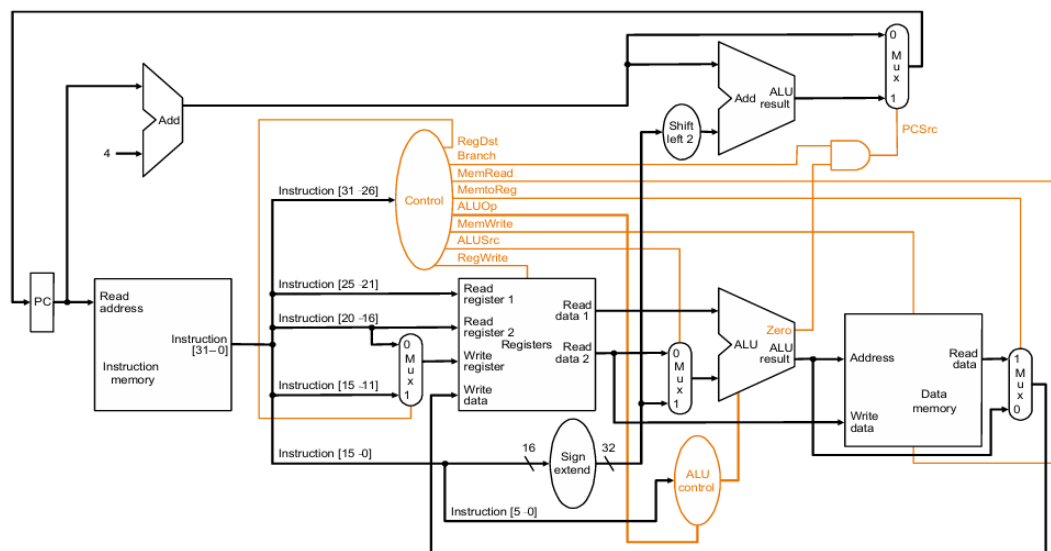


組別：_____ 簽名：_____

[group 1]

1. Consider the datapath shown below. Give the values of RegDst, ALUSrc, MemtoReg, RegWrite, MemRead, and MemWrite when executing

(a) add \$12, \$13, \$14 (b) lw \$12, 4(\$13) (c) sw \$12, 4(\$13) (d) addi \$12, \$13, 14



Ans:

- (a) RegDst=1, ALUSrc=0, MemtoReg=0, RegWrite=1, MemRead=0, MemWrite=0
- (b) RegDst=0, ALUSrc=1, MemtoReg=1, RegWrite=1, MemRead=1, MemWrite=0
- (c) RegDst=x, ALUSrc=1, MemtoReg=x, RegWrite=0, MemRead=0, MemWrite=1
- (d) RegDst=0, ALUSrc=1, MemtoReg=0, RegWrite=1, MemRead=0, MemWrite=0

x denotes “don’t care”

[group 2]

2. True/False (T/F)

1. In the Register File, the clock signal (CLK) is a factor ONLY during a write operation. During a read operation, it behaves like a combinational circuit.
2. According to the idealized memory model described in the slides, both read and write operations require a clock (CLK) signal, and a "MemRead" control signal is necessary to enable a read operation.
3. In a single-cycle implementation, the clock period is determined by the longest-delay instruction (e.g., lw). This Critical Path includes the PC's Clk-to-Q delay, Instruction Memory Access Time, Register File Access Time, ALU delay, Data Memory Access Time, and the Register File Setup Time.
4. The single-cycle clocking methodology allows a value to be read from a state element, processed by combinational logic, and written back to the same state element all within the same clock cycle.
5. When executing a lw (load word) instruction, the "ALUSrc" control signal should be set to 0, allowing the ALU to operate on the contents of registers rs and rt.

Ans:

1. T
2. F (The CLK is only a factor during a write operation, and no read control signal is needed.)
3. T
4. F (The slides state there is "no feedback within a single cycle".)
5. F (For lw, ALUSrc must be 1 to select the sign-extended immediate value as the second ALU input.)

[group 3]

3. What is the order of designing a processor?

- A. Analyze instruction set (data path requirements)
- B. Assemble the control logic
- C. Select set of data path component and establish clocking methodology
- D. Assemble data path meeting the requirements
- E. Analyze implementation of each instruction to determine setting of control points effecting register transfer

Ans: a -> c -> d -> e -> b

[group 5]

4. Which of the following statements about a single-cycle MIPS processor design are true or false?

- a. In a single-cycle processor design, the clock cycle time is determined by the longest delay path among all instructions.
- b. The "shamt" field in the R-type instruction is used to specify the target address for jump instructions.
- c. The program counter (PC) is updated to $PC + 4$ for every instruction in the MIPS subset described.
- d. The register file has two read ports and one write port, allowing two registers to be read and one to be written in the same cycle.
- e. In a single-cycle implementation, the same instruction is executed over multiple clock cycles.

Ans:

- a. True
- b. False (The "shamt" field is used for the shift amount, not for jump addresses.)
- c. False (For branch instructions like *beq*, the PC may be updated to a different address.)
- d. True
- e. False (In a single-cycle design, each instruction is completed in one clock cycle.)

[group 6]

5. Question:

True or False

- a. When processing R-type instructions, the clock period should be set to accommodate the longest delay among R-type instructions.
- b. We cannot decide all control signals by op-code.
- c. We can use funct of R-Type instruction as the ALU select signal directly to decrease design complexity.
- d. The ALU Zero output signal is only used by branch instructions.

Ans:

- a. False, it should be set to the longest delay among all instructions, if not pipelined
- b. True, an example is that we need funct field in R-Type
- c. False, we reuse the ALU in different type of instructions, and we use a ALU control to generate the control signal
- d. True, The Zero output from the ALU indicates whether the ALU result is zero. This signal is primarily used by branch equal (beq) instructions to determine if two registers are equal.

[group 10]

6. Question:

What happens if the clock period is too long or too short?

Ans:

If the clock period is too long:

The circuit runs slower. It's stable and reliable, but performance and throughput decrease.

If the clock period is too short:

Timing violations may occur, causing wrong data to be latched. The processor may behave unpredictably or fail.

[group 11]

7. True or False:

- (a) In a MIPS single-cycle processor, both instruction memory and data memory can be accessed in the same clock cycle.
- (b) In a single-cycle processor, the generation time of control signals does not affect instruction execution time, as control signals and data flow occur in parallel.
- (c) In the MIPS instruction set, the branch target address is calculated by shifting the immediate field left by 2 bits and adding it to the program counter (PC).
- (d) The execution time of a single-cycle processor is determined by the slowest instruction, meaning the load instruction delay determines the clock cycle time.

Ans:

- (a) Answer: True Explanation: In a single-cycle MIPS design, instruction memory and data memory are separate. This allows the processor to fetch an instruction and perform a load/store operation in the same clock cycle.
- (b) Answer: False Explanation: The generation of control signals does affect execution time because the control signals must be generated before the data can be correctly routed through the datapath.
- (c) Answer: False Explanation: In MIPS, the branch target address is computed by shifting the immediate value left by 2 bits (since MIPS instructions are word-aligned) and adding it to the $PC + 4$.
- (d) Answer: True Explanation: In a single-cycle processor, the clock cycle time must be long enough to accommodate the slowest instruction (typically the load instruction), which determines the overall clock period.

[group 13]

8. True or False. Give your reasoning for false answers

- a) Combinational logic elements produce outputs that depend only on the current inputs, not on any stored information.
- b) If the only thing a processor needs to do is fetch consecutive instructions, the cycle time would depend only on the speed of the instruction memory.
- c) In an edge-triggered clocking methodology, all state changes occur only at a clock edge, such as the rising edge.
- d) Before assembling a processor's control logic, the datapath must be designed to support all register transfers implied by the instruction set.
- e) In a single-cycle processor design, each instruction has a different clock cycle length depending on how long it takes to execute.

Ans:

a) ~~True~~ (False, input can from stored informaiton)

b) ~~False~~ True

~~We cannot rely only on the instruction memory, because the cycle time depends on the longest delay in the entire combinational logic path.~~

c) True

d) True

e) False

It uses one fixed clock cycle for all instructions because the clock cycle must be long enough to accommodate the slowest instruction.

[group 14]

9. Question:

What instruction below may fail to run correctly if the control signal “RegDst” in the single-cycle CPU has been cut and stuck at 1?

(1) add

(2) sw

(3) lw

(4) slt

Ans: (3)

[group 8]

10. Question:

True or False

- A. In basic logic design, information is encoded in binary, and one wire carries a whole word.
- B. In a register file, we can read two data values and write one into the register file, or read one and write two, depending on the program.
- C. In a single-cycle CPU, the control point is the MUX, and all control signals are generated only by the control unit.
- D. Edge-triggered means that the stored value updates when the clock changes from 1 to 0

(or 1 to 0).

Ans:

- A. F: One wire carries one bit, not a whole word.
- B. F: We can only read two data values and write one into the register file. This behavior is determined by hardware design, not by the program.
- C. F: reference p42 , Not only the main control unit manipulates control signals. For example, the PC source signal depends on both the control unit and the ALU's result (for branch decisions). There is also a separate ALU control unit.
- D. T ~~-F: Edge triggered means the stored value updates on the rising edge (0→1 transition) of the clock.~~

[group 7]

11. Question:

Explain why processors use a clock signal instead of allowing logic to operate continuously.

Ans:

The clock acts as a global timing reference that synchronizes all parts of the processor. Each clock cycle defines when data can safely move between registers and logic units. All computations must complete within a clock cycle; otherwise, when data is transferred, it may still be unstable or mid-computation, leading to incorrect results.