Computer Architecture

Fall, 2025
Week 8
2025.09.20

組別：_____ 簽名：_____

[group 1]

1. Qustion:

(Floating Point Representations)

In the IEEE 754 single-precision floating-point format, what is the largest possible unbiased exponent value that can be represented by a normalized number? (Exclude the all-ones exponent reserved for ∞ and NaN).

Ans:

[group 2]

2. Question:

Suppose that A = 0xB and B = 0x7. Show the step-by-step result of multiplying A and B, using Booth's algorithm. Assume A and B are 4-bit two's complement integers, stored in hexadecimal format. When is it not ideal to implement Booth's algorithm?

Ans:

[group 5]

3. Question:

State T/F and explain briefly.
a. On MIPS, **Lo holds quotient, Hi holds remainder**.
b. `div` **automatically** raises and handles divide-by-zero in hardware.
c. **Divide HW V2** uses **shift-left remainder** (not shift-right divisor).
d. In signed division, the **remainder follows the dividend's sign**.
e. Integer multiply and divide **share** the same ALU/shift hardware (direction and add/sub differ).

Ans:

[group 7]

4. Question:

1) Interpret the following **double-precision** bit pattern as a decimal number
0 **1**00000000**1**0 **1**0**1**0000000000000000000000000000000000000000000000000000

Ans:

[group 8]

5. Question:

True or False?

(A) Floating point representation consist of only three part: sign, exponent and fraction.
(B) Use 2's complement on exponent representation.
(C) IEEE 754 preserve encodings for " Infinity", " NaN". However, it fails to represent "denormalized numbers".
(D) The precision of floating-point is relative precision depending on the exponent part of floating-point

Ans:

[group 9]

6. Question:

Why is the exponent in floating-point representation not represented using two ‘s complement, but instead represented using biased notation?

Ans:

[group 6]

7. Question:

True or False:

a. when we use mult $t1, $t2, we will push most significant 32 bits to lo and least significant 32 bits to hi.

b. In biased 15, 10110 represents 7.

c. Hi and Lo registers are used in both multiplication and division, and Hi would store the quotient in division.

d. Exponents with all 1’s are reserved for ±∞ and NaN.

e. When performing signed division, it can first be treated as unsigned (positive) division.

Ans:

[group 10]

8. Question:

why the syntax [mult] only use two registers as operands? Please describe the difference between [mult] with [mul].

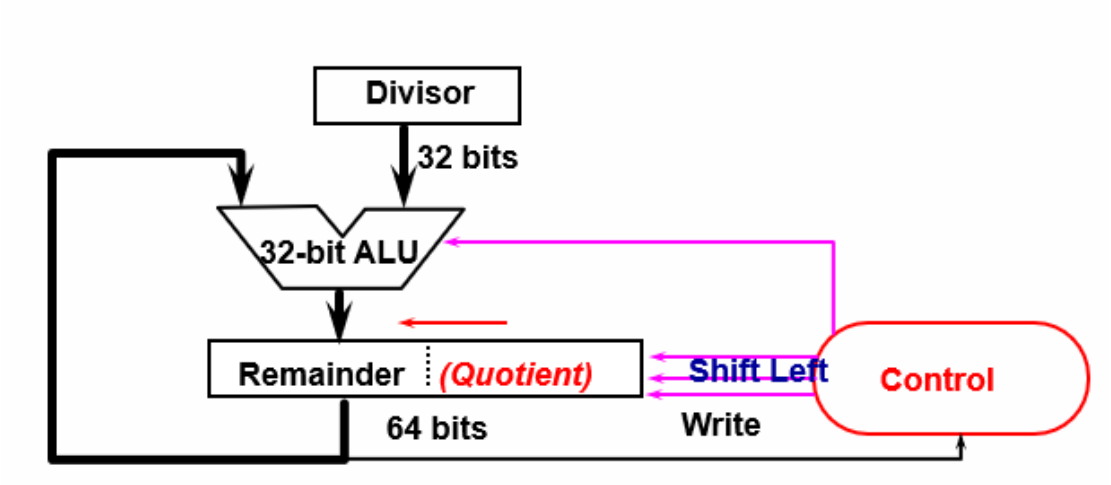
Ans. Since mult may have an result of 64-bits which need 2 special reg (hi lo) to store. However, mul directly store the least significant 32-bits in the destination register.

Ans:

[group 12]

9. Question:

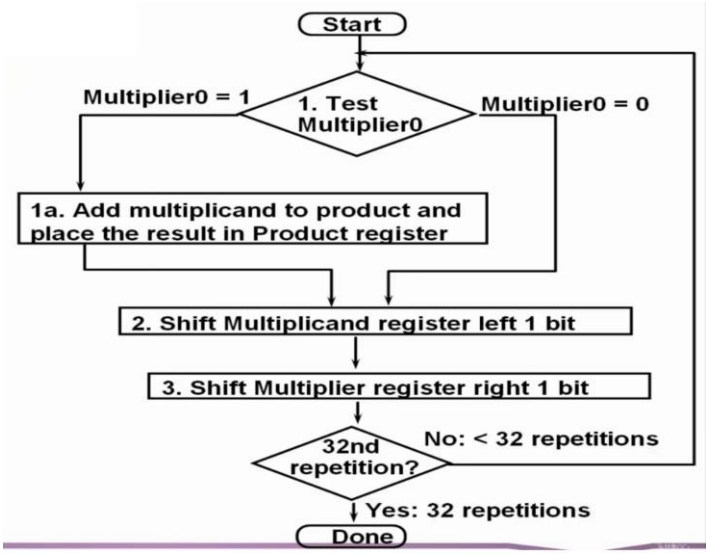
Given the divisor below (unsigned), we perform 0111/0011. Please write down the value in the remainder for every step.



Ans:

[group 3]

10. Question:



Using the flowchart above, we are implementing the multiplication 1100 × 0101.

Assume that after one ALU operation (step 1a) is completed, the content of the Multiplier register is 0001. What is the content of the Product register at this moment?

Ans:

[group 14]

11. Question:

Write down the IEEE 754 representation (in hex format) for the value "-13.125_{10}"

Ans: