Computer Architecture

Fall, 2025
Week 10
2025.11.03

組別：_____ 簽名：_____

[group 7]

1. Explain the differences between a **single-cycle processor** and a **pipelined processor**. In your answer, include:

a) How each processor executes instructions.

b) When pipelining is preferred and when a single-cycle processor may be used instead.

c) The **main weaknesses** of both processors.

Ans:

Execution method:

- **Single-cycle processor:** Executes **one instruction per long clock cycle**. Each instruction goes through all five stages (IF, ID, EX, MEM, WB) in a single cycle.
- **Pipelined processor:** Splits instruction execution into **multiple stages**, allowing **different instructions to be processed simultaneously** in separate pipeline stages — improving **throughput**.

When to use:

- **Pipelining** is used in **modern CPUs** where **high instruction throughput** is required (e.g., desktops, servers).
- **Single-cycle** designs are used in **simple, low-power systems** (like small embedded processors or teaching processors) where simplicity is more important than speed.

Weaknesses:

- **Single-cycle processor:**
    - Very **long clock period** determined by the slowest instruction.

- **Hardware underutilization** — most functional units stay idle part of the time.

- **Pipelined processor:**
  - **Complex control** and **hardware overhead** (needs pipeline registers, hazard detection, forwarding).
  - Suffers from **pipeline hazards** (data, control, structural) that can cause **stalls** or reduced performance.

[group2]

2. What makes pipelining easy in MIPS?

Ans:

1) All instructions are of the same length.

2) Just a few instruction formats.

3) Memory operands only in loads and stores.

[group 8]

3. When implementing pipelined control, why should we store rt and rd in our pipeline registers

Ans:

It is because the selection of write register happens in the Wr stage, while the instruction decoding and register file read is on a previous stage. Therefore, since we cannot access rt and rd during the Wr stage, we have to carry this information along.

[group 2]

4. Answer the following question:

1) What are the **five stages** of the MIPS pipeline?

2) In which stage are registers **read** / **written**?

3) In which stage does the **ALU** operate?

Ans:

1) IF – Instruction Fetch

ID – Instruction Decode / Register Fetch

EX – Execute / ALU Operation

MEM – Memory Access

WB – Write Back

2) Read → ID stage (Instruction Decode stage)

Write → WB stage (Write Back stage)

3) The ALU performs arithmetic and logical operations in the EX stage.

[group 3]

5. Give the correct order of the datapath stage:

A: MEM(data memory access)

B: ID(instruction decode and register file read)

C: WB(write back)

D: IF(instruction fetch)

E: EX(execution or address calculation)

Ans: DBEAC

[group 5]

6. If a pipelined process has 5 stages and takes 100 ns to execute N instructions. How long will it take to execute 2N instructions, assuming the clock rate is 500 MHz and no pipeline stalls occur?

Ans:

Clock cycle time = $1/(500*10^6)$ = 2ns,

N+4 = 100 ns = 50 clock cycle -> N takes 46 cycle

2N = [46*2+4(cycle)]*2(ns) = 192 ns

[group 6]

7. True or False

a) If each instruction is divided into five stages with equal delay, we can expect pipelining to be five times faster than a single-cycle processor.

b) Clock period is determined by slowest stage in pipelined processor.

c) We cannot complete an instruction during one clock cycle if we split an instruction into multiple stages.

d) For one instruction, unlike a single-cycle processor, pipelined control signals (excluding ALUctr) are generated in different stages and used in different stages too.

Ans:

a) False. Some resource has no task at the first few and last few cycles. Five times faster is ideal but not in practice.

b) True. The clock period (time of one clock cycle) must be long enough to allow the slowest pipeline stage to complete its work.

c) True. An instruction completes when all stages done, it needs more than one cycle.

d) False. All control signals are generated in the same stage (ID stage).

[group 10]

8. If pipelining doesn't make a single instruction faster, then why do we still say that pipelining improves processor performance?

Ans:

Pipelining improves throughput, not latency. By overlapping the execution of multiple instructions, the CPU can complete one instruction every clock cycle after the pipeline is full. So even though each instruction isn't faster individually, more instructions are completed per unit time, which increases overall performance.

[group 11]

9. True or False.

a) Pipelining decreases the time it takes to complete a single task
b) Pipelining improves overall throughput when processing multiple tasks
c) In a non-pipelined system, all stages of the process are working concurrently
d) The speed-up from pipelining is proportional to the number of stages in the pipeline

Ans:

a) False: in pipelining, the time to complete one task remains the same because each task still passes through every stages

b) True: pipelining allows multiple tasks to be worked simultaneously at different stages, leading to faster overall completion of many tasks, which improves throughput

c) False: in a non-pipelined system, only one task is being worked at a time. Each stage waits of the previous stage to finish before starting (tasks are completed sequentially)

d) True: if all stages take roughly the same amount of time and the pipeline is full, the speed-up is proportional to the number of stages. For example, a pipeline with five stages can complete five tasks in the time it would take a non-pipelined system to complete one

[group 5]

10. Assume that a single cycle datapath with the critical path of 10 ns can be partitioned into arbitrary number of balanced stages for pipelining, and there is no dependency between instructions. If the pipelining will introduce an additional 1 ns delay to each stage. What is the speedup for the 4-stages pipelined datapath when compared with the single-cycle one? (a long sequence of independent instructions so that the 4-stage pipeline is fully utilized)

Ans:

The instruction time for a single-cycle machine = 10 ns

The instruction time for pipeline = (10/4)+1 = 3.5 ns

Speedup = 10/3.5 = 2.86

[group 14]

11. Assume that individual stages of the datapath have the following latencies:

IF	ID	EX	MEM	WB
300ps	400ps	350ps	500ps	100ps

1) What is the clock cycle time for a pipelined processor and a single-cycle processor?

2) What is the total latency of the lw instruction for a pipelined processor and a single-cycle processor?

Ans:

1) Pipelined: 500ps; Single-cycle: 1650ps

2) Pipelined: 2500ps; Single-cycle: 1650ps