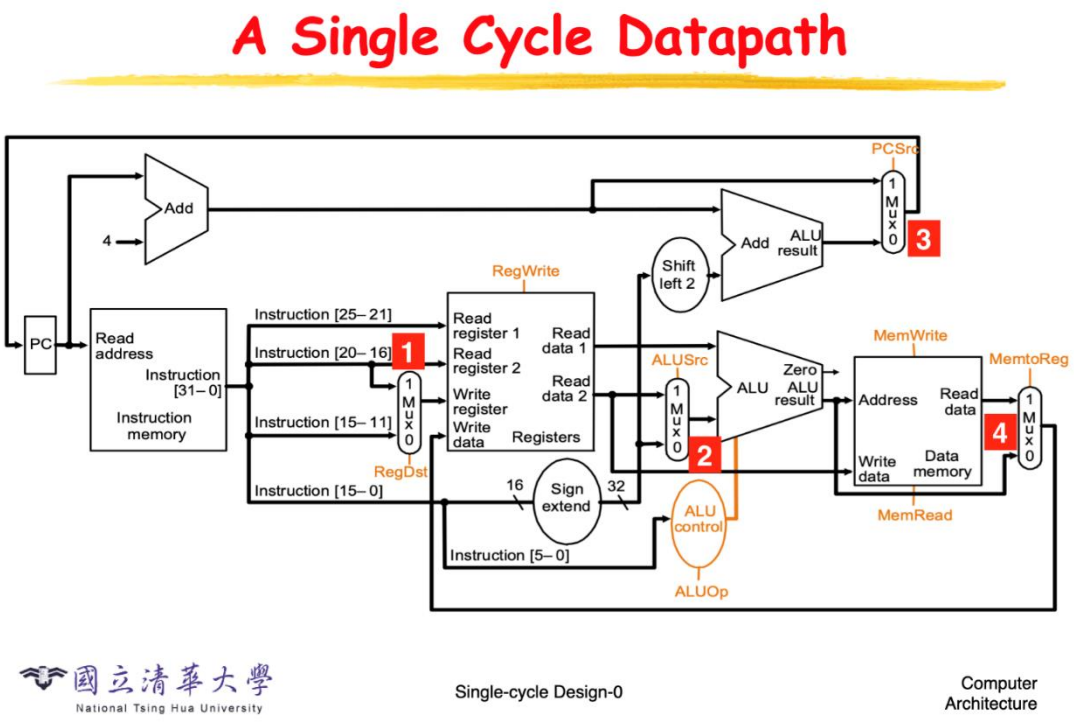
Computer Architecture

Fall, 2024
Week 9
2024.10.28

組別：_____ 簽名：_____

[group 3]

1. 按照圖中處理器的設計，在 add, bne, lw 三種情況下，四個 MUX 的值是什麼



Ans:

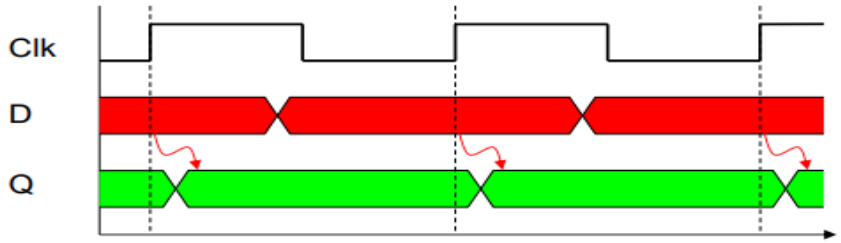
add: 0, 1, 1, 0

bne: x, 1, 0(由 zero 決定), x

lw : 1, 0, 1, 1

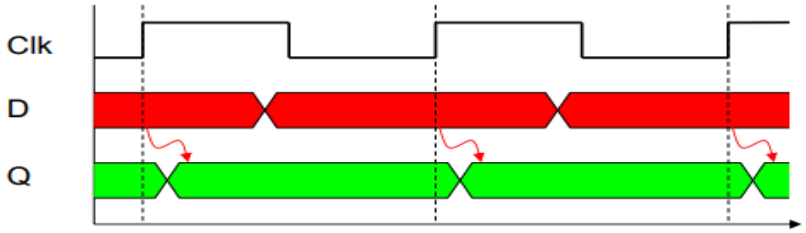
[group 5]

2. 說明什麼是 Edge-triggered ？ 請圈出發生 Edge-triggered 的時刻



Ans:

Edge-triggered：update when Clk changes ~~from 0 to 1~~



[group 7]

3. 0pcode 經過 controller 的處理後可以決定大部分的 control signals，但有哪兩個例外？請分別說明它們如何運作。

Ans:

1. PCSrc

   執行前須經過一個 AND gate 接收兩個 input

   (1) controller: branch instruction

   (2) ALU: 表示 rs 和 rt 中的值是否相等，1 代表 branch condition 成立

   AND gate output = 1 時 PC 會跳到 target address

2. ALUop (ALUctr generated by ALUop and functional field)

R-Type 需要知道 functional field 才知道 ALU 要做什麼 operation

[group 9]

4. 是非題

(a) In a MIPS single-cycle processor, both instruction memory and data memory can be accessed in the same clock cycle.

(b) In a single-cycle processor, the generation time of control signals does not affect instruction execution time, as control signals and data flow occur in parallel.

(c) In the MIPS instruction set, the branch target address is calculated by shifting the immediate field left by 2 bits and adding it to the program counter (PC).

(d) The execution time of a single-cycle processor is determined by the slowest instruction, meaning the load instruction delay determines the clock cycle time.

(e) In the MIPS single-cycle processor datapath, the ALU's "Zero" signal is only used during arithmetic operations.

Ans:

(a) **Answer: True**
Explanation: In a single-cycle MIPS design, instruction memory and data memory are separate. This allows the processor to fetch an instruction and perform a load/store operation in the same clock cycle.

(b) **Answer: False**
Explanation: The generation of control signals does affect execution time because the control signals must be generated before the data can be correctly routed through the datapath.

(c) **Answer: False**
Explanation: In MIPS, the branch target address is computed by shifting the immediate value left by 2 bits (since MIPS instructions are word-aligned) and adding it to the PC + 4.

(d) **Answer: True**
Explanation: In a single-cycle processor, the clock cycle time must be long enough to accommodate the slowest instruction (typically the load instruction),

which determines the overall clock period.

(e) **Answer: False**
Explanation: The ALU's "Zero" signal is also used in branch instructions, such as beq, to determine if two register values are equal, influencing whether a branch is taken.

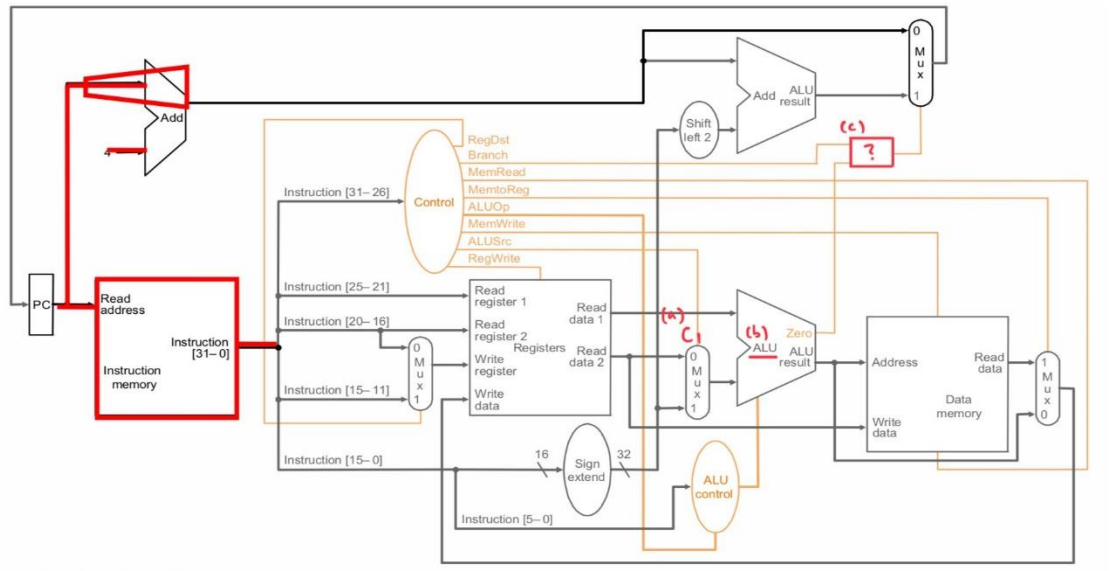
[group 11]

5. When the instruction is beq (Branch if Equal),

a) what should the control signals C1 be?

b) what operation should the ALU do?

c) Additionally, which logic gate should be used at the location marked with the red question mark in the diagram to determine whether the program counter (PC) should branch?



Ans:

(a) C1: 0
(b) sub
(c) AND gate

[group 1]

6. What are the key components required to implement branch instructions like BEQ in a single-cycle datapath?

Ans:
To implement branch instructions like BEQ (branch if equal) in a single-cycle datapath, the following components are required:

1. ALU (Arithmetic Logic Unit): To compare the values of the two registers involved in the branch (e.g., $t0 and $t1).
2. Program Counter (PC): Stores the address of the current instruction and will be updated either to the next sequential instruction or the branch target address.
3. Adder: To compute the branch target address. This is done by adding the sign-extended, left-shifted branch offset to the value of PC + 4.
4. Sign Extender: Extends the immediate field of the branch instruction (which is 16 bits) to a 32-bit value.
5. Shift-left-2 unit: Shifts the sign-extended branch offset left by 2 to account for word alignment (each instruction is 4 bytes).
6. Multiplexer (MUX): To choose between PC + 4 (next sequential instruction) or the branch target address, depending on the outcome of the ALU comparison.
7. Control Unit: Generates control signals for the ALU, PC update logic, and MUX selection, ensuring that the branch is taken only if the comparison condition is met (for BEQ, if the two registers are equal).

[group 2]

7. The followings are the steps for how to design a processor. Please write down the steps in the correct order.

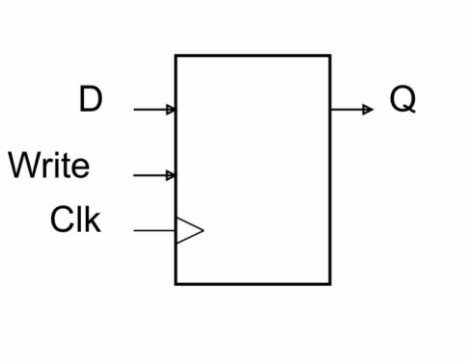
(A) Select set of datapath components and establish clocking methodology
(B) Analyze instruction set
(C) Assemble the control logic
(D) Analyze implementation of each instruction to determine setting of control points effecting register transfer
(E) Assemble datapath meeting the requirements

Ans:

(B) -> (A) -> (E) -> (D) -> (C)

[group 4]

8. 請問附圖的 element 什麼時候會 update



Ans:

only updates on clock edge when write control input is 1

[group 6]

9. True or False

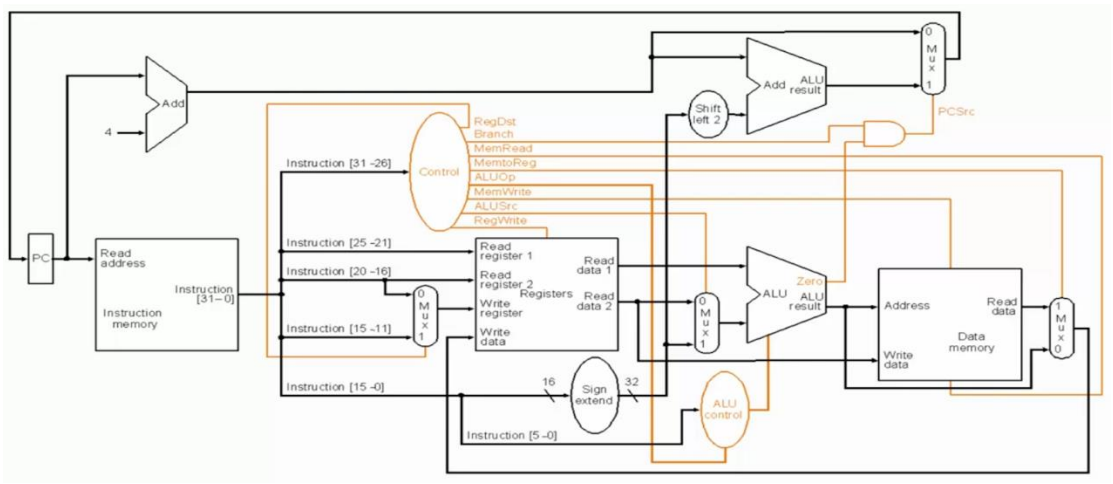
1. In a MIPS single-cycle processor, every instruction takes the same amount of time to execute.
2. The program counter is updated during instruction execution to point to the next instruction in a single-cycle processor.
3. In MIPS, an instruction fetch and a memory access can occur simultaneously in a single cycle.
4. In a single-cycle MIPS processor, the ALU can only perform addition operations.

Ans:

(1) True. In a single-cycle design, each instruction completes in one clock cycle.
(2) True. The PC is typically updated to point to the next instruction(sequentially).
(3) True. This is a characteristic of the single-cycle architecture.
(4) False. The ALU can perform operations including subtraction, AND, OR …

[group 10]

10. According the following datapath:



The time cost of every steps are as follow:

a. fetch/renew PC number: 4ms
b. adder: 2ms
c. instruction decode: 8ms
d. register read/write: 6ms
e. every multiplexer/AND gate: 1ms
f. sign extend: 1ms
g. shift left 2: 1ms
h. every ALU operation: 6ms
i. memory read/write: 8ms
j. ignore connection cost (the lines in graph)
k. ignore time cost on generating and sending control signal

Please calculate how much time does the processor need to operate add, lw?

Ans:

a. add

add operation: PC(4) + instruction decode(8) + mux(1) + register read(6) + mux(1) + ALU(6) + mux(1) + register write(6) = 33ms

pc renew: PC(4) + instruction decode(8) + sign extend(1) + shift left 2(1) + ALU(6) + mux(1) + renew PC(4) = 25

so time cost dominated by add operation: 33ms(ans)

b. lw

lw operation: PC(4) + instruction decode(8) + mux(1) + register read(6) + mux(1) + ALU(6) + memory read(8) + mux(1) + register write(6) = 41

pc renew: same as above

so time cost dominated by lw operation: 41ms(ans)

[group 12]

11. Please review the following statements, and provide corrections for those that are wrong

A) ALUOp control signal determines what operation the ALU should perform
B) When MemRead is 1, data is written to memory
C) RegWrite = 1 indicates a register write operation is needed
D) Branch signal alone determines whether to take a branch
E) MemtoReg selects between ALU result or memory data to write back to register

Ans:

Correct statements: A, C, E
Incorrect statements:

- **B is incorrect**: When MemRead = 1, data is read from memory, not written. (MemWrite controls writing to memory)
- **D is incorrect**: The Branch decision requires both the Branch signal and the ALU Zero output (Branch AND Zero for beq, Branch AND NOT Zero for bne)