Computer Architecture

Fall, 2024
Week 6
2024.10.08

組別：_____ 簽名：_____

[group 1]

1. 問答題

How many MUX are in ALU, what are their purposes?

Ans:

Two for selecting inputs to the ALU. For example, for subtraction, one of the inputs might need to be negated. One for selecting which operation's result should be output based on the control signal.

[group 2]

2. Overflow may occur when:

(a) positive number - positive number

(b) positive number - negative number

(c) negative number - positive number

(d) negative number - negative number

(e) positive number + positive number

(f) positive number + negative number

(g) negative number + negative number

Ans: (b), (c), (e), (g)

[group 3]

3. 問答題

In the MIPS instruction set, what is the difference in behavior between the add and addu instructions when adding two numbers that cause an overflow? Which situation triggers overflow handling and which does not?

Ans:

The add instruction checks for overflow when adding signed numbers. If an overflow occurs, it triggers an exception, saving the current program counter (PC) to the exception program counter (EPC) and jumping to an exception handler.

In contrast, the addu instruction does not check for overflow when adding unsigned numbers. Even if there is an overflow, it simply wraps around without triggering any

exception. Therefore, add is used when overflow needs to be checked, while addu is used when overflow is not a concern.

[group 4]

4. 是非題 (錯誤請說明原因)
   a) We can use sub and its signed bit to implement 'set on less than' in hardware.
   b) MIPS addu and addi instructions ignores overflow.
   c) When an exception occurs the PC is saved into the EPC register.

Ans:

(a) 正確。在硬體中，我們可以使用「sub」指令和其帶有符號的位元（signed bit）來實現「set on less than」操作。

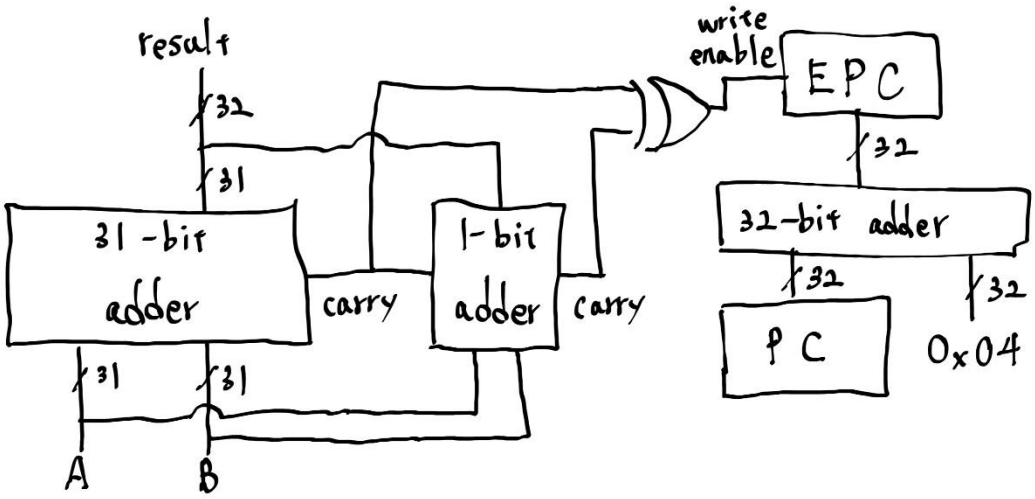
(b) 錯誤。
ignore overflow: addu, addui, subu
Don't ignore overflow: add, addi, sub

(c) 正確。當例外事件發生時，PC（Program Counter）的值會被保存到 EPC（Exception Program Counter）中。

[group 5]

5. Draw a diagram with n-bit adders, PC, EPC, and necessary logic gates to implement the overflow detection mechanism with EPC.
   (Only illustrate the relevant components and connections for this mechanism.)

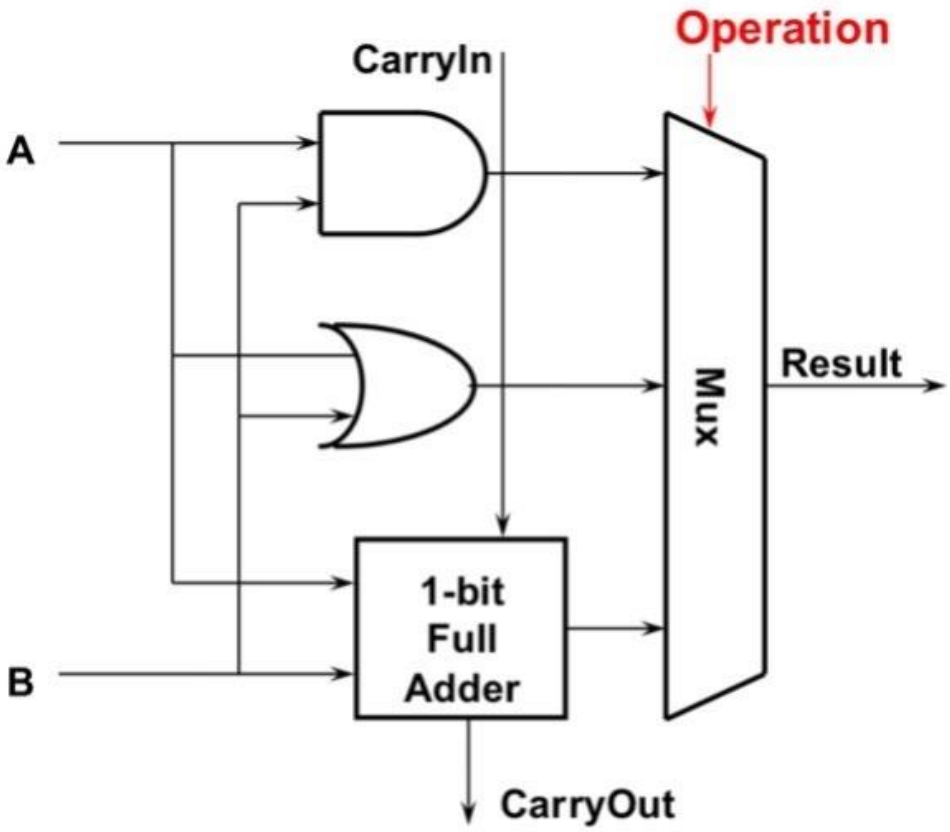
Ans:



EPC 存 PC 而非 PC+4

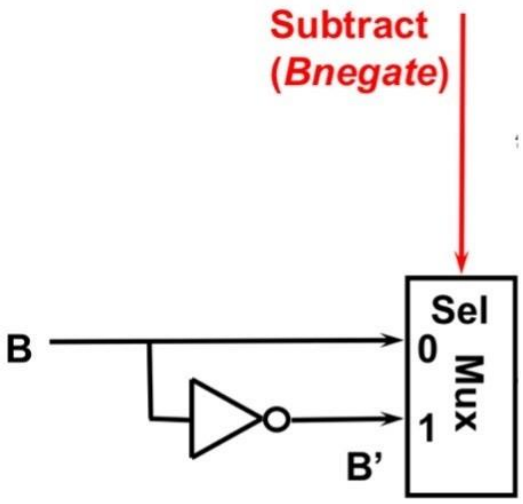
[group 6]

6. 下圖為一個 1-bit ALU，若想要在上面添加減法功能，需要怎麼實現？並請說明 2’complement 如何實作減法。



Ans:

2’complement 要實作 A-B 可以用 A+(B’+1)來計算得出，因 B’+1 的值會等於-B。因此需要再原本 ALU 的 B 前面增加一個 MUX，為了不要破壞原本既有的功能，需要增加一個 control line，當其值為 1 時，才將 B 做 bit-wise negation，同時再將 LSB 的 carry in 設為 1。



[group 7]

7. Compare the gate delay of two 4-bits adder, one implement with Ripple Carry Adder, the other with Carry Lookahead Adder. (Assume each logic gate has one gate delay)

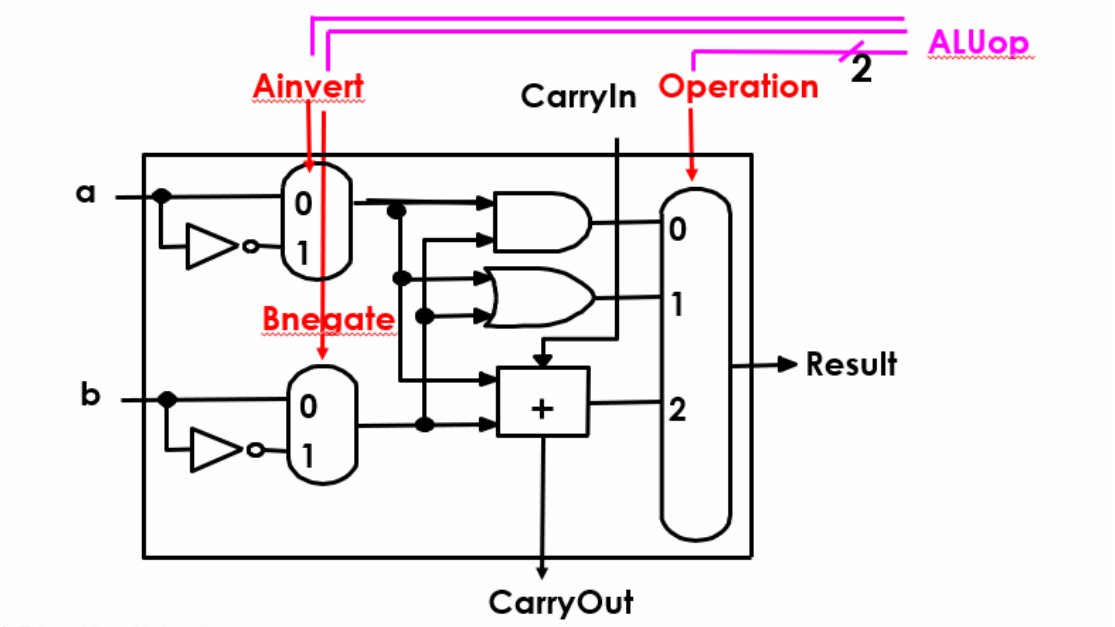
Ans:

ripple-carry-adder: 4 * 2 = 8

carry lookahead adder: 1 + 2 = 3

[group 11]

8. Base on the following design, what is the equivalent logic gate when the ALU control signal is set to 1101?



Ans: (not A) or (not B) is equivalent to NAND gate

[group 14]

9. For these 4-bit signed number, which of them are overflow?
   a) 0010+1010
   b) 1111+1000
   c) 0011+0111
   d) 1010+0100

Ans: b, c

[group 9]

10. You have a 4-bit ALU that can perform addition, subtraction, AND, OR, and SLT operations. The input ALUcode is 0111. Given A=0110 and B=1100 , what will the result of the operation be?

Ans:

The ALU code correspond to SLT operation.

A = 0110 = $(6)_{10}$

B = 1100 = $(-4)_{10}$

Because A > B so the result of the operation is 0

(應該會進 exception)

[group 12]

11. 是非題 (錯誤請說明原因)
    a) We can detect overflow in ALU by using XOR gate.
    b) ALUOP 0000 is the control signal of add.
    c) We can implement NOR with AND gate and inverters in ALU.
    d) The operation of slt is subtract two input numbers and output the result of sign bit in ALU.

Ans:

a) T
b) F 0010
c) T
d) T