

CS4100 Computer Architecture

Fall, 2024

Outlines (Sep. 2)

Week 1 (9/2)	Introduction Ch1-1 Computer: A historical perspective, abstractions (10:03) (page 1-12)	
Week 2 (9/9) 助教： 林承賢	Chapter 1: Computer Abstractions and Technology Ch1-2.1.1 Technology - Performance (1) (11:09) (page 13-21) Ch1-2.1.2 Technology - Performance (2) (11:08) (page 22-31) Ch1-2.2 Power trends, measuring performance, cost (13:32) (page 32-49)	H1: Bench- marking
Week 3 (9/16) 助教： 王睿杰	Chapter 2: Instruction Set Architecture Ch2-1 Instruction set architecture (5:15) (page 1-6) Ch2-2.1 Operands - Register operands and their organization (13:37) (page 7-14) Ch2-2.2.1 Operands - Memory operands, data transfer (1) (11:19) (page 15-21) Ch2-2.2.2 Operands - Memory operands, data transfer (2) (8:27) (22-26) Ch2-2.3 Operands - Immediate operands (6:04) (page 27-31)	
Week 4 (9/23) 助教： 唐梧遷	Ch2-4 Representing instructions (19:30) (page 32-43) Ch2-5.1 Operations - Logical (10:47) (page 44-54) Ch2-5.2 Operations - Decision making and branches (15:55) (page 55-63)	H2:(MIPS) if-then-else, loop inst.
Week 5 (9/30) 助教： 林承賢	Ch2-6.1 Supporting procedures in hardware (1) (16:01) (page 64-74) Ch2-6.2 Supporting procedures in hardware (2) (10:11) (page 75-79) Ch2-7 Communicating with people (4:00) (page 80-83) Ch2-8 Addressing for 32-bit addresses (15:31) (page 84-94) Ch2-9 ARM and x86 instruction sets (10:12) (page 95-103)	H3:(MIPS) procedure call, recursive call
Week 6 (10/7) 助教： 王睿杰	Chapter 3: Computer Arithmetic Ch3-1 Add, sub, and, or, nor (11:44) (page 1-14) Ch3-2.1 SOLT, overflow detection, zero detection (13:58) (page 15-26) Ch3-2.2.1 Cascaded carry look ahead adder (12:42) (page 27-35) Ch3-2.2.2 Multiple level carry look ahead adder (7:44) (page 36-43)	
Week 7 (10/14) 助教： 唐梧遷	Ch3-3.1 Unsigned multiply (18:47) (page 44-54) Ch3-3.2 Signed multiply (13:41) (page 55-60) Ch3-4 Division (21:35) (page 61-72) Ch3-5.1.1 Floating point representations (1) (15:48) (page 73-85) Ch3-5.1.2 Floating point representations (2) (8:34) (page 86-99) Ch3-5.2 Floating point addition and multiplication (15:26) (page 100-111)	
Week 8 (10/21)	Midterm exam , 1:20 – 3:10 PM, Chaps 1-3	

Week 9 (10/28) 助教： 林承賢	Chapter 4: Designing a Single-Cycle Processor Ch4-1 Introduction to designing a processor (15:19) (page 1-12) Ch4-2 Analyzing the instruction set (10:08) (page 13-17) Ch4-3 Buliding the datapath (14:34) (page 18-28) Ch4-4 A single cycle implementation (8:51) (page 29-34) Ch4-5.1 Control of CPU operations (10:19) (page 35-45)	
Week 10 (11/4) 助教： 王睿杰	Ch4-5.2 ALU controller (9:26) (page 46-57) Ch4-6 Main controller and jump instruction (10:33) (page 58-68) Chapter 5: Pipelining Ch5-1 An overview of pipelining (9:52) (page 1-8) Ch5-2 A pipelined datapath (15:21) (page 9-33) Ch5-3 Pipelined control (7:31) (page 34-51)	
Week 11 (11/11) 助教： 唐梧遷	Ch5-4 Hazard: types of hazards (8:23) (page 52-58) Ch5-5-1 Handling data hazard Inserting NOP (4:56) (page 59-62) Ch5-5-2 Handling data hazard Forwarding, R Type use (13:48) (page 63-73) Ch5-5-3 Handling data hazard Stall, load use (10:51) (page 74-82)	
Week 12 (11/18) 助教： 林承賢	Ch5-6 Handling branch hazards (10:23) (page 83-92) Ch5-7 Exceptions (7:17) (page 93-101) Ch5-8 Superscalar and dynamic pipelining (19:38) (page 102-119)	
Week 13 (11/25) 助教： 王睿杰	Chapter 6: Memory Hierarchy Ch6-1 Memory hierarchy (14:32) (page 1-10) Ch6-2-1 Basics of caches - Direct mapped cache (11:46) (page 11-26) Ch6-2-2 Basics of caches - Address sub division (10:33) (page 27-34) Ch6-2-3 Basics of caches - Cache hit and miss (6:32) (page 35-40)	Project: (C/C++) Cache
Week 14 (12/2) 助教： 唐梧遷	Ch6-2-4 Basics of caches - Memory support (9:01) (page 42-47) Ch6-3 Measuring cache performance (6:36) (page 48-53) Ch6-4-1 Improveing cache performance - Set associative cache (17:00) (page 54-65) Ch6-4-2 Improveing cache performance - Multiple level cache (9:19) (page 66-72) Ch6-5-1 Virtual memory - Basic (10:33) (page 73-80)	
Week 15 (12/9) 助教： 林承賢	Ch6-5-2 Virtual memory - Issues in virtual memory (13:44) (page 81-90) Ch6-5-3 Virtual memory - Handling huge page table and TLB (11:20) (page 91-100) Ch6-5-4 Virtual memory - TLB and cache (9:37) (page 101-105) Ch6-6 A common framework for memory hierarchy (11:27) (page 106-114)	
Week 16 (12/16)	Final exam , 1:20 – 3:10 PM, Chaps 4-6	