Computer Architecture

Fall, 2023

Week 13

2023.12.04

組別：_____ 簽名：_____

[group1]

1. Select the correct statements

a. We can reduce the delay of a taken branch by moving branch execution earlier from MEM to IF.

b. There are two kinds of unexpected events, exception arising from an external I/O controller and interrupt from CPU.

c. With dynamic prediction, we have a one cycle penalty for a branch taken. (with history table and branch target buffer)

d. With the prediction, we don’ t need to know the target address of branch.

e. In MIPS with static dual issue, it puts load/store instruction after ALU/branch in two issue packets.

Ans:

a. False. IF -> ID. We can't fetch data in registers to compare in IF stage

b. False. There are two kinds of unexpected events, exception arising from CPU and interrupt from an external I/O controller.

c. True.

d. False. We still need to calculate the target address of branch in prediction

e. True.

[group4]

2. For each of the following techniques, determine whether it is associated primarily with a compiler approach, a hardware approach, or both.

A. Multiple issue

B. Very Long Instruction Word

C. Out-of-order execution

Ans:

A. both

B. software-based

C. hardware-based

[group2]

3. True or False?

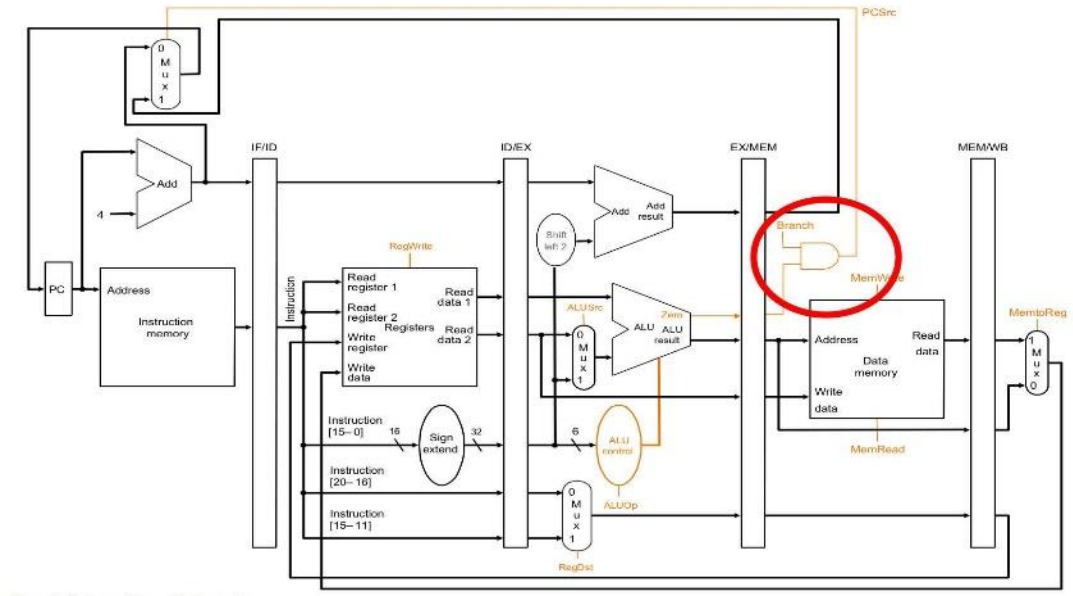
(a) To increase Instruction-Level Parallelism, the CPU can group instructions to create Very Long Instruction Words (VLIWs).

(b) The two instructions:
sub $2, $6, $9
sw $2, 0($6)
can be grouped into a dual issue packet.

(c) Dynamic Scheduling is a must, whereas Static Scheduling is a plus.

(d) Given 3 instructions in a single-issue pipeline:
add $2, $6, $9
lw $9, 0($2)
add $9, $9, $2
sw $2, 0($6)
If we can rearrange the order of the instructions, we can achieve an optimal IPC of 0.5.
(forwarding and stalling can both be utilized)

(e) Consider the pipeline processor design shown below:



If “branch equal” is taken, 3 instructions that have entered the pipeline will have to be flushed (changed to NOPs) to make up for the prediction mistake.

Ans:

(a) False, ~~CPU~~ → compiler

(b) False, there is dependency between the two instructions

(c) False, not must

(d) True, we can achieve IPC = 4/8 by switching the order of the 2^{nd} & 3^{rd} instruction.

(e) True

[group12]

4. Choose the correct statement(s).

(a) When handling branch hazards with static prediction, we predict branch always not taken.

(b) When handling hazard in deeper pipelines and superscalar pipelines, less cycle loss is generated since the design of hardware is more flexible.

(c) After the conditional selection, we fetch the target address if the branch isn't taken. (without prediction)

(d) Although we have the predictor, we still need to find the target address so that we generate 2 additional cycle penalties.

(e) Unexpected events occurring in the CPU are called exception.

Ans:

(a) true

(b) false. In deeper and superscalar pipelines, more cycle loss is generated.

(c) false. We fetch the target address if the branch is taken.

(d) false. 1-cycle penalty for a taken branch.

(e) true

[group6]

5. True or false

(a) pipeline stalling can be used to solve all 3 types of hazards

(b) exception handling uses much of the same hardware as control hazard handling, only difference being exception handling needs to flush the entire pipeline to accommodate handler codes

(c) deeper pipeline can result in an IPC > 1

(d) despite hardware being more rigid than software, compiler is not mainly used for dynamic multiple issue

Ans:

(a) True

(b) False: only flush current and subsequent instructions

(c) False: deeper pipeline -> more speedup; multiple-issue -> CPI < 1

(d) True

[group9]

6. Please choose the correct statements.

A. Dynamic pipeline scheduling allows the CPU to execute instructions and commit result to registers out of order to avoid stalls.

B. Cache misses are unpredictable at compile time.

C. Pipelining is independent of technology.

D. There are two types of unexpected events. Interrupt arises within the CPU and exception arises from an external I/O controller.

E. In MIPS, exceptions managed by a System Control Coprocessor (CP0).

Ans: B E

A: Dynamic pipeline scheduling allows the CPU to execute instructions out of order to avoid stalls, but it commits result to registers in order.

C: Pipelining is dependent on the technology.

D: Exception arises within the CPU and interrupt arises from an external I/O controller.

[group14]

7. What is the order of the following steps when dealing with exceptions in pipeline before jumping to OS?

A. Flush the offending and subsequent instructions

B. Set Cause and EPC register values

C. Stop the offending instruction

D. Transfer control to handler

E. Complete the previous instructions

Ans:

C -> E -> A -> B -> D

[group7]

8. Choose the correct answer and correct the wrong one.

(A) After jumped to OS, no matter what the problem is, the program would be terminated.

(B) Exception can be seen as another form of data hazard.

(C) There is no dependency between packets, but possibly some dependencies with a packet.

(D) We can use NOP to solve the dependency problem between packets.

Ans: D

(A) After jumped to OS, if the problem is restartable, the corrective action would be taken; otherwise, the program would be terminated.

(B) Exception can be seen as another form of control hazard.

(C) There is no dependency with a packet, but possibly some dependencies between packets.