Computer Architecture

**Fall, 2023**

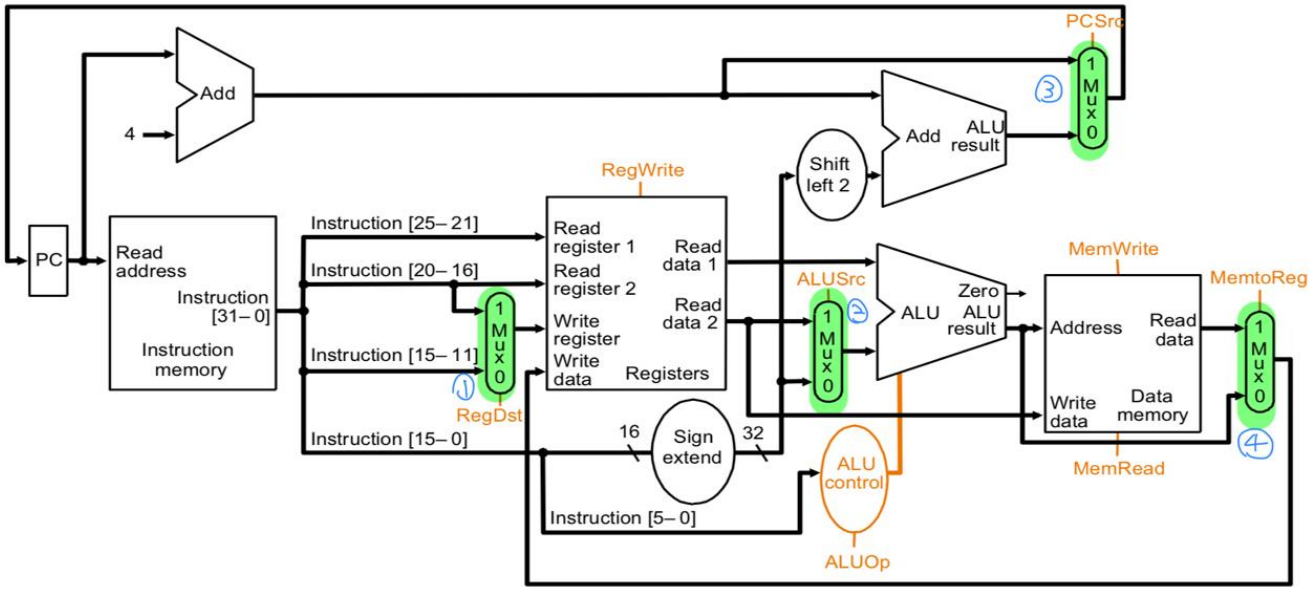
**Week 9**

**2023.11.13**

**組別：_____ 簽名：_____**

[group13]

1. What are these four MUX used for? (Need to explain what happens when control is one or zero.)




Ans:

(1) It is used to choose “write register “. When Control is 1, we write data in “rt” (is lw instruction), when control is 0, we write data in “rd” (is R-type instruction)

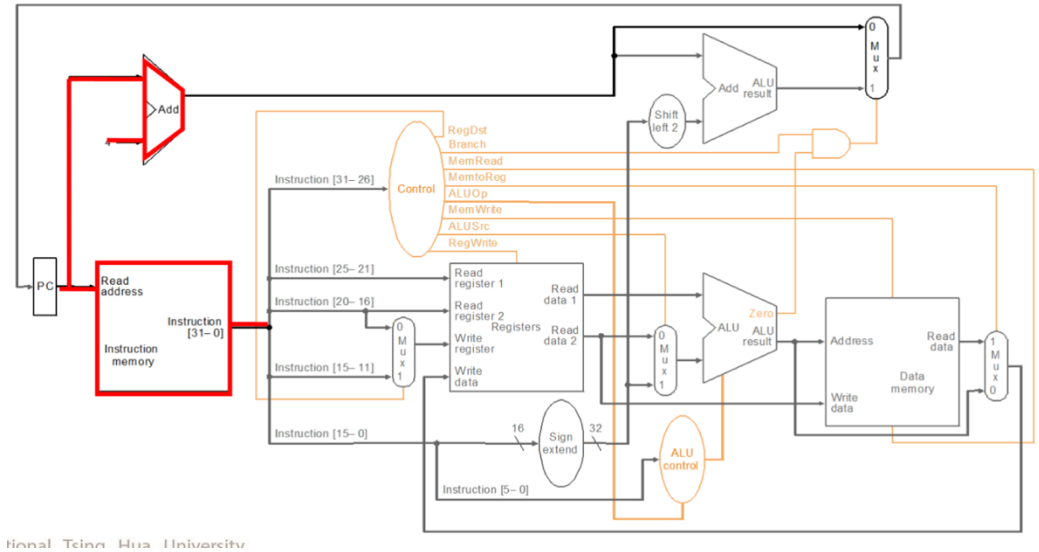
(2) It is used to choose “immediate “or “read data2”. When Control is 1, we choose “read data2” in to ALU (is add, sub or beq instruction), when control is 0, we choose “immediate” in to ALU (is the constant of “addi” or the offset of “lw” instruction)

(3) It is used to choose where PC go to. When Control is 1, PC will be PC+4, when control is 0, PC will be PC+4+signExt[imm16] *4 (is “beq” instruction).

(4) It is used to choose which data go back to the register. When Control is 1, the data is “read data of memory “( lw instruction), when control is 0, the data is ALU result (add, addi or sub instruction).

[group5]

2. For the instructions below, what should be the output of the controller?



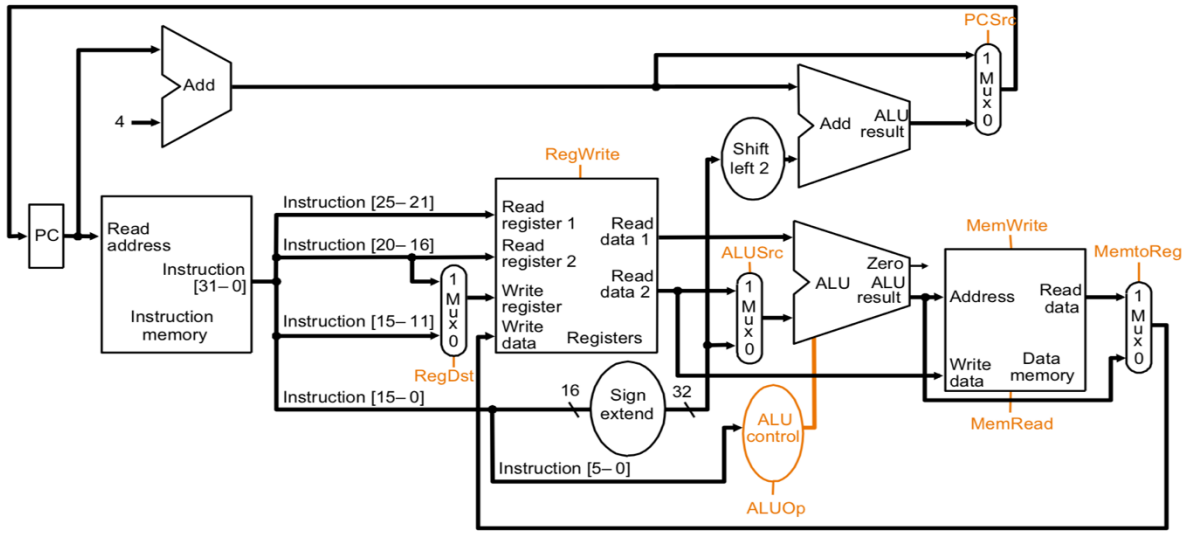

Ans:

| Instruction | add | lw | beq |
|---|---|---|---|
| RegDst | | | |
| Branch | | | |
| MemRead | | | |
| MemtoReg | | | |
| MemWrite | | | |
| ALUSrc | | | |
| RegWrite | | | |

| Instruction | add | lw | beq |
|---|---|---|---|
| RegDst | 1 | 0 | doesn’t matter |
| Branch | 0 | 0 | 1 |
| MemRead | 0 | 1 | 0 |
| MemtoReg | 0 | 1 | doesn’t matter |
| MemWrite | 0 | 0 | 0 |
| ALUSrc | 0 | 1 | 0 |
| RegWrite | 1 | 1 | 0 |

[group8]

3. Assume the latency of instruction memory, add, mux, ALU, register, data memory, control and sign extend are respectively 450ps, 100ps, 40ps, 130ps, 200ps, 350ps, 110ps, 40ps.




(1) What's the latency of the critical path for a MIPS ADD instruction?

(2) What's the latency of the critical path for a MIPS LW instruction?

(3) What's the latency of the critical path for a MIPS BEQ instruction?

Ans:

(1) 450+200+40+130+40+200 = 1060ps

(2) 450+200+130+350+40+200 = 1370ps

(3) 450+200+40+130+40 = 860 ps

[group7]

4. True or false, and explain why.
   A. For lw and add instruction, the control signals for RegDst must be different.
   B. It is possible to determine PCSrc only with opcode.
   C. If opcode = 0, MemtoReg can be determined right away.
   D. Read data 1,2 depend on different instruction bits for lw and add.
   E. Instruction[13] can be one of the input bits for Sign extend or Write register.

Ans:

   A. True. Because the destination of lw is rt and the destination of add is rd, their control signals must be different.
   B. False. PCSrc depends on ALU zero and Branch.
   C. True. Opcode = 0, then it must be an R type instruction. So MemtoReg = 0, which selects the result of ALU instead of the data from memory.
   D. False. Read data 1,2 take the same bits (instruction[25-21], instruction[20-16]) as Read registers for both lw and add.
   E. True. For R type instructions, instruction[15-11] is rd, which is the input for Write register. For I type instructions, instruction[15-0] is the input of Sign extend.

[group6]

5. What is the order of the following steps when designing a processor?
   (a) Assemble datapath meeting the requirements.
   (b) Select the set of datapath components and establish the clocking methodology.
   (c) Assemble the control logic.
   (d) Analyze instruction set (data requirements).
   (e) Analyze implementation of each instruction to determine setting of control points effecting register transfer.

Ans:

   (d)(b)(a)(e)(c)

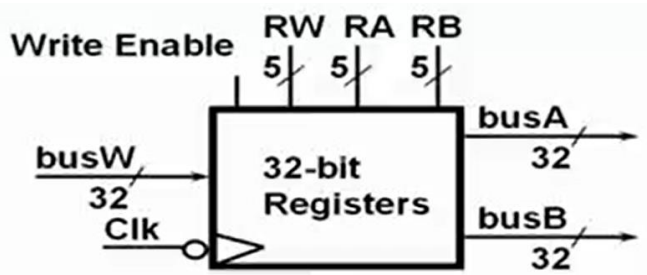
[group9]

6. Answer the following questions:

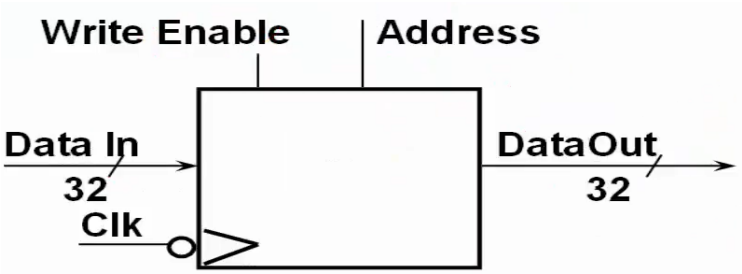
(a) How to determine clock period?

(b) In the "fetch instruction" stage, we can determine what type of instruction to execute. Therefore, we do not read all fields during the "read register" phase. True or False?

(c) Why do RA, and RB need 5 bits, and what is the purpose of the Write enable? Explain.




(d) What are the differences between the Write enable in the lower diagram and the Write enable in the upper diagram?




Ans:

(a) 根據 combinational logic 最長的 data path(longest delay)去決定

(b) False, "After the 'fetch instruction' stage, there are actually three formats for an instruction: R type, I type, and J type. Therefore, during the read register phase, all fields are read in. Once the instruction is decoded, the opcode will indicate which type of instruction to use."

(c) Because we use RA and RB to determine whether Bus A or Bus B reads from which register, and there are 32 registers, so we need 5 bits to represent this. Used to control whether to write in each clock cycle.

(d) The “Write Enable” in the lower diagram determines whether to perform a write operation or a read operation.

[group3]

7. Please decide whether the following statements are true or false.
   A. In a single-cycle processor, the Program Counter (PC) is only updated at the beginning of the execution of a new program.
   B. The Arithmetic Logic Unit (ALU) in a single-cycle processor is used exclusively for arithmetic operations and does not perform logical operations.
   C. The control unit generates control signals that remain constant throughout the execution of all types of instructions.
   D. Single-cycle processors complete the execution of each instruction in exactly one clock cycle.
   E. Data memory in a single-cycle processor is used to store the results of arithmetic and logic operations from the ALU.

Ans:

   A. False. The Program Counter (PC) is updated to point to the next instruction at the end of the execution of the current instruction, not only at the beginning of a new program.
   B. False. The ALU performs both arithmetic and logical operations, not just arithmetic operations.
   C. False. The control unit generates control signals that vary depending on the particular instruction being executed, as different instructions require different control signals.
   D. True. Single-cycle processors are designed to complete the execution of each instruction in exactly one clock cycle.
   E. False. Data memory is used to store and retrieve data used by the program, not to store the results of ALU operations. The results of ALU operations are typically stored in registers within the CPU.

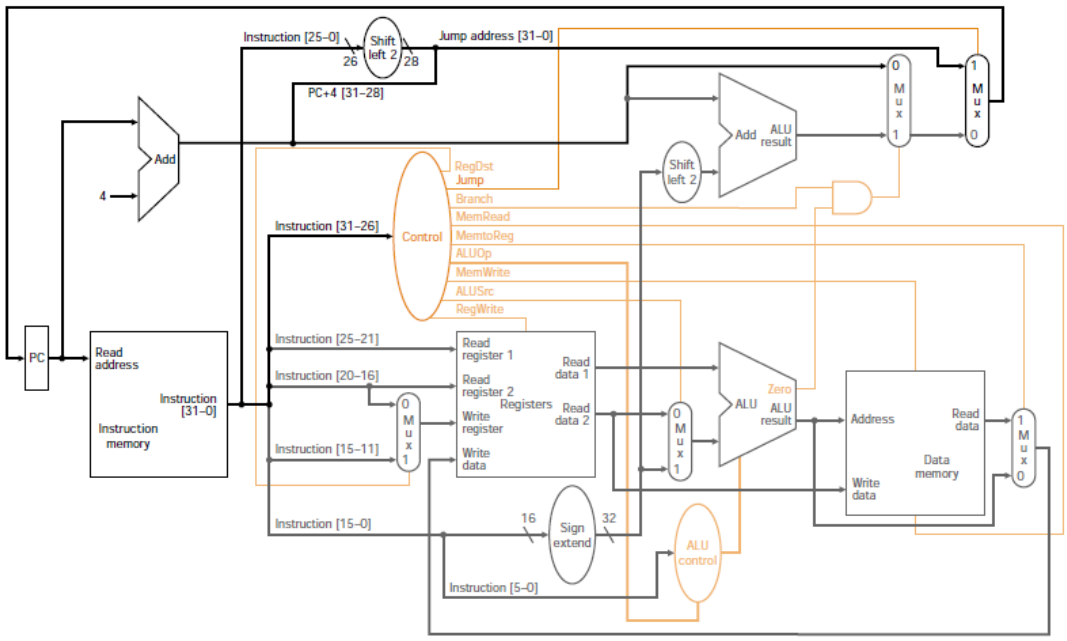
[group10]

8. Control signal below is NOT a signal from the existing MIPS ISA. Determine the functionality of the signal in the given datapath. Assume the ALUctrl is 0110 (subtract). (You don't need the information of ALUOp for this problem.) We denote this custom I-type instruction as: ABC $rs, $rt, imm16.

Control signal:

| name | RegDst | Jump | Branch | MemRead | MemtoReg | ALUOp | MemWrite | ALUSrc | RegWrite |
|---|---|---|---|---|---|---|---|---|---|
| value | 0 | 0 | 1 | 0 | 1 | ALUctrl is given | 1 | 1 | 0 |

Datapath:




Ans:

This instruction branches to PC + 4 + imm16*4 if rs == imm16. Additionally, store rt into address rs - imm16 in memory.