## A Simple Machine Language

Sep 22, 2009

## The Machine's Architecture

- 16 general-purpose registers - numbered 0 through F (in hexadecimal)
- Each register is
- one byte (8 bits) long
- assigned
to represent its
register number
- E.g.

0000 (0x0) -> register 0
0100 (0x4) -> register 4

## The Machine's Architecture (Cont.)

$\triangleleft$ Main memory

- 256 memory cells
- Each cell is located by an integer $\diamond$
- Floating-point values are stored in the eight-bit format disscussed in Section 1.7 and summarized in Figure 1.26


## The Machine's Language

- Machine language
- two bytes ( 16 bits) long
- op-code field -> leftmost 4 bits
- operand field -> the remaining 12 bits


## Simulator (Java version)

| CPU |  |  |  |
| :--- | :--- | :--- | :--- |
| R0 | 00 |  |  |
| R1 | 00 |  |  |
| R2 | 00 |  |  |
| R3 | 00 |  |  |
| R4 | 00 |  |  |
| R5 | 00 |  |  |
| R6 | 00 |  |  |
| R7 | 00 | PC | 00 |
| R8 | 00 | IR | 0000 |
| R9 | 00 |  |  |
| RA | 00 |  |  |
| RB 00 |  |  |  |
| RC | 00 |  |  |
| RD | 00 |  |  |
| RE | 00 |  |  |
| RF | 00 |  |  |


|  | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 1 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 2 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 3 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 4 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 5 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 6 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 7 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 8 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 9 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| A | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| B | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| C | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| D | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| E | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| F | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |


| Clear Memory | Load Data | Run | Single Step | Halt | Help |
| :---: | :---: | :---: | :---: | :---: | :---: |

## Example

$\diamond$ From Questions \& Exercises

- Suppose the memory cells at addresses B0 to B8 in the machine described in Appendix C contain the (hexadecimal) bit patterns given in the following table:

| Address | Contents |
| :---: | :---: |
| B0 | 13 |
| B1 | B8 |
| B2 | A3 |
| B3 | 02 |
| B4 | 33 |
| B5 | B8 |
| B6 | C0 |
| B7 | 00 |
| B8 | OF |

## Example (Cont.)

a. If the program counter starts at B0, what bit pattern is in register number 3 after the first instruction has been executed?

## Syntax

## [PC] B0 <br> [B0] 13 B8 A3 02 33 B8 C0 00 0F



## Load Data



## Load Data (Cont.)

| (8imple Computer |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\square$ | X |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Data Input Window |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| $\begin{aligned} & {[\mathrm{PC}] \mathrm{B0}} \\ & {[\mathrm{BO}] 13 \mathrm{~B} 8 \mathrm{~A} 30233 \mathrm{~B} 8 \mathrm{C} 0000 \mathrm{~F}} \end{aligned}$ |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| CPU | Main Memory |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| R0 00 | 0 |  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |  |
| R1 00 | 0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |  |
| R2 00 | 1 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |  |
| R3 00 | 2 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |  |
| R4 00 | 3 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |  |
| R5 00 | 4 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |  |
| R6 00 | 5 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |  |
| R7 00 PC B0) | 6 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |  |
| R8 00 IR 0000 | 7 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |  |
| R9 00 | 8 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |  |
| RA 00 | 9 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |  |
| RB 00 | A | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |  |
| RC 00 | B | 13 | B8 | A3 | 02 | 33 | B8 | C0 | 00 | OF | 00 | 00 | 00 | 00 | 00 | 00 | 00 |  |
| RD 00 | C | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |  |
| RE 00 | D | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |  |
| RF 00 | E | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |  |
|  | F | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |  |
|  | Clear Memory |  |  | Load Data |  |  | Run |  | Single Step |  | Halt |  | Help |  |  |  |  |  |

## The Result of Sub-problem a



## Example (Cont.)

b. What bit pattern is in memory cell B8 when the halt instruction is executed?

## The Result of Sub-problem b



