

#### CS4101 嵌入式系統概論

# **Analog-to-Digital Converter**

Prof. Chung-Ta King Department of Computer Science National Tsing Hua University, Taiwan

Materials from *MSP430 Microcontroller Basics*, John H. Davies, Newnes, 2008



# **Recall the Container Thermometer**

- Container thermometer: monitor the temperature of the interior of a container
  - Monitor the temperature every 5 minutes
  - Flash LED alarm at 1 Hz
  - If the temperature rises above a threshold, flash the LED alarm at 3 Hz and notify backend server
  - If the temperature drops below a threshold, return the LED alarm to normal and notify the server

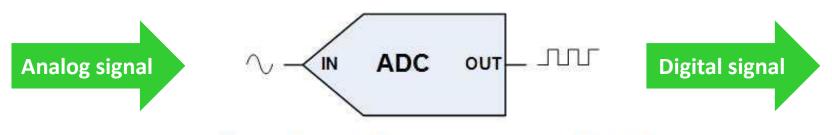


#### **Need to know the temperature!**



#### **Digitizing Temperature**

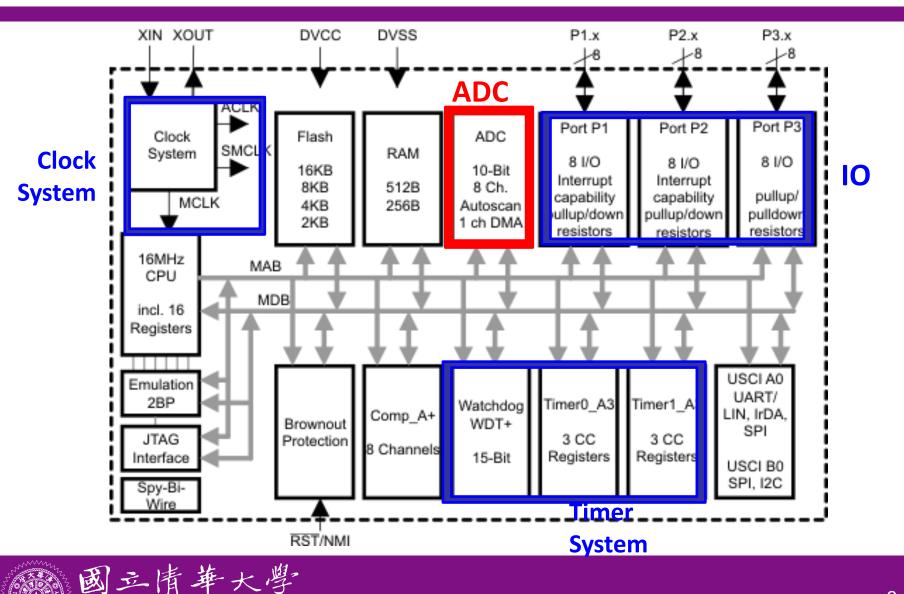
- Temperature is a nature phenomena, whose value vary continuously
- To make it feasible for computer to handle, we need to convert it into digital signals
- To transform an analog signal into a digital one, the *analog-to-digital converter* (ADC) samples the input at fixed interval and do the conversion



ELECTRICAL SYMBOL FOR ANALOG TO DIGITAL CONVERTER (ADC)



#### We Have Learned ...



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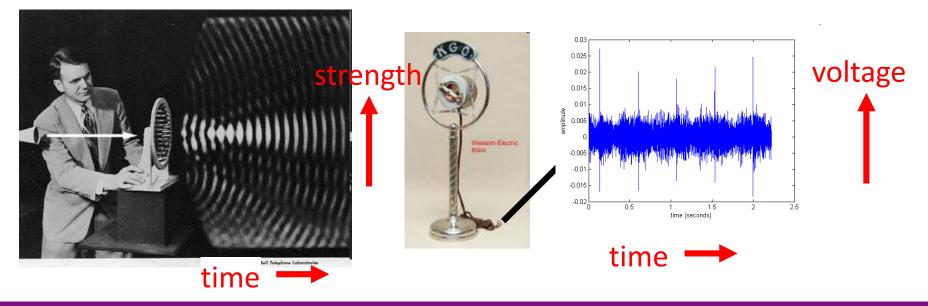


- Introduction to analog-to-digital conversion
- ADC of MSP430
- Sample code of using ADC10 in MSP430



## **Analog Signals**

- A signal representing continuous things, e.g.
  - Fluctuations in air pressure (i.e. sound) strike the diaphragm of a microphone, which causes corresponding fluctuations in a voltage or the current in an electric circuit
  - The voltage or current is an "analog" of the sound



#### **Analog-to-Digital Conversion**

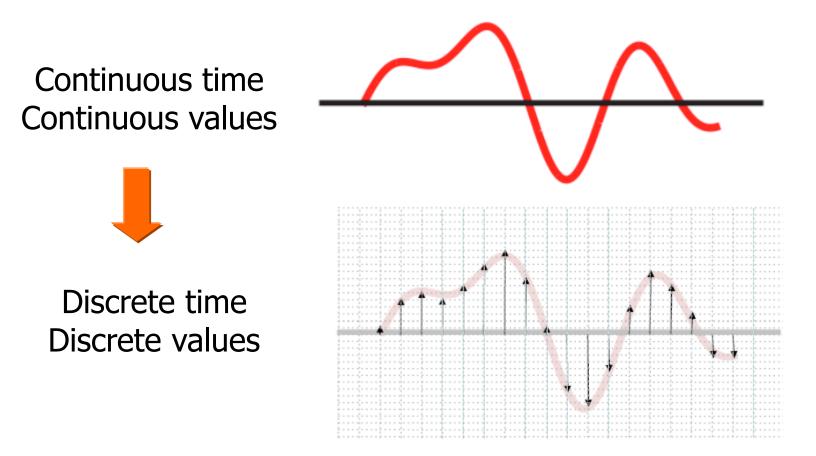
- ADC: convert an analog input, e.g., a voltage V, into a binary value that the processor can handle
  - The input V(t) is a continuous function, i.e., V can take any value within a permitted range and can change in any way as a function of time t
  - The output V[n] is a sequence of binary values. Each has a fixed number of bits and can represent only a finite number of values.
  - Typically input is sampled regularly at intervals of Ts, so the continuous nature of time has also been lost.

Of course, we also have DAC (digital-to-analog converter)!



#### **Analog-to-Digital Conversion**

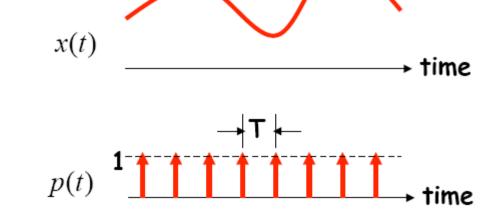
Digital representations of analog waveforms

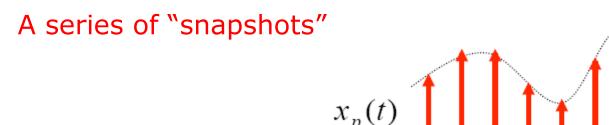




# Sampling in Time

 The value of the analog signal is measured at certain intervals in time. Each measurement is referred to as a sample





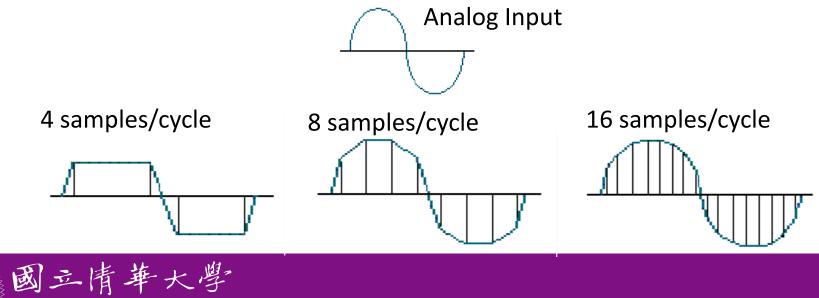


### **Terminologies in Sampling**

- Sampling rate:
  - How often analog signal is measured (samples per second, Hz), e.g. 44,100 Hz?
- Sampling resolution:

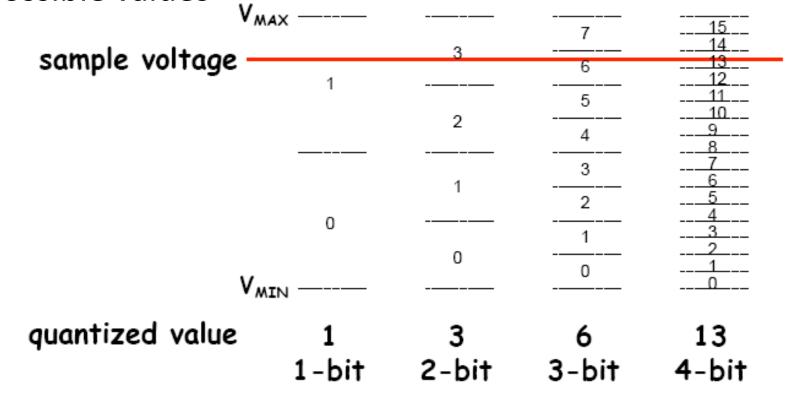
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 Number of bits to represent each sample ("sample word length," "bit depth"), e.g. 16 bit



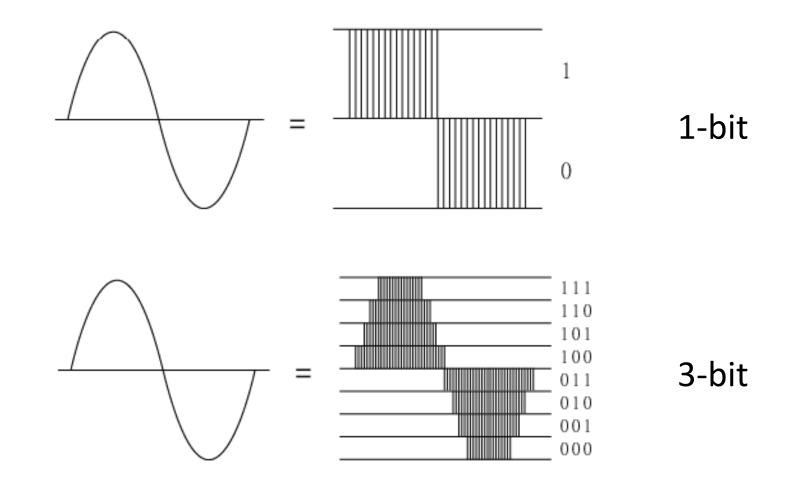
#### **Encoding of Discrete Signals**

 If we use N bits to encode the magnitude of one of the discrete-time samples, we can capture 2<sup>N</sup> possible values





#### **Sampling Rate and Encoding Bits**





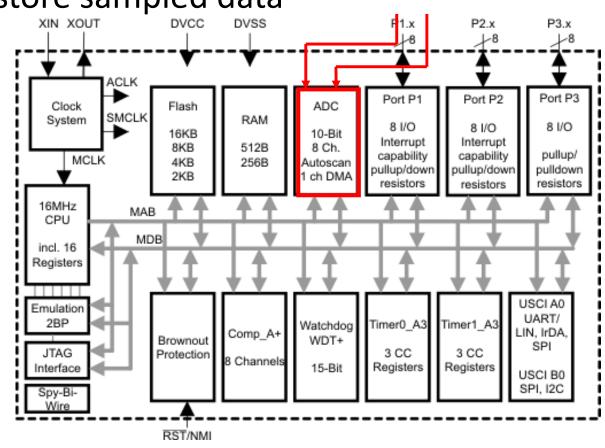


- Introduction to analog-to-digital conversion
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 Provide continuous sampling of multiple analog inputs and store sampled data

- ADC10AE0
- INCH in ADC10CTL1





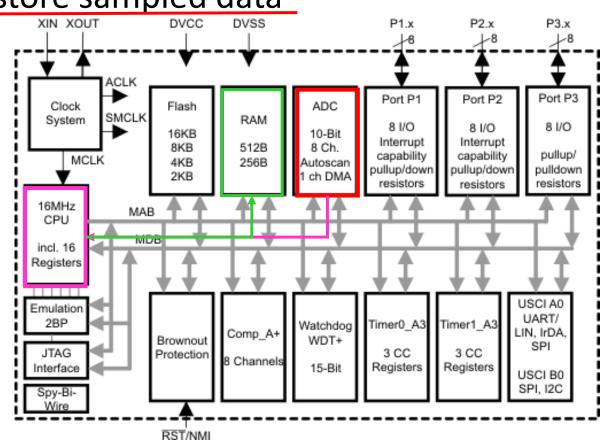
- Provide continuous sampling of multiple analog inputs and store sampled data
- P2.x DVCC DVSS P1.x XIN XOUT P3.x 1-8 1-8 ACLK Port P2 Port P3 Port P1 Clock Flash ADC RAM System SWOLD 8 I/O 8 I/O 8 I/O 16KB 10-Bit SHS, ADC10SSEL, Interrupt Interrupt 8KB 8 Ch. 512B capability capability pullup/ MCLK 256B 4KB Autoscan pullup/down pulldown pullup/down **CONSEQ** in 2KB ch DMA resistors resistors resistors 16MHz MAB ADC10CTL1 CPU MDB incl. 16 Registers USCI A0 Emulation UART/ 2BP Timer0 A3 Timer1 A3 Watchdog Comp\_A+ LIN, IrDA. Brownout WDT+ SPI 3 CC 3 CC JTAG Protection 8 Channels Registers Registers 15-Bit Interface USCI B0 SPI, I2C Spy-Bi-Wire RST/NMI



 Provide continuous sampling of multiple analog inputs and <u>store sampled data</u>

Interrupt CPU on every word sampled from ADC

Use software (ISR run by the CPU) to move data from ADC (ADC10MEM) to memory

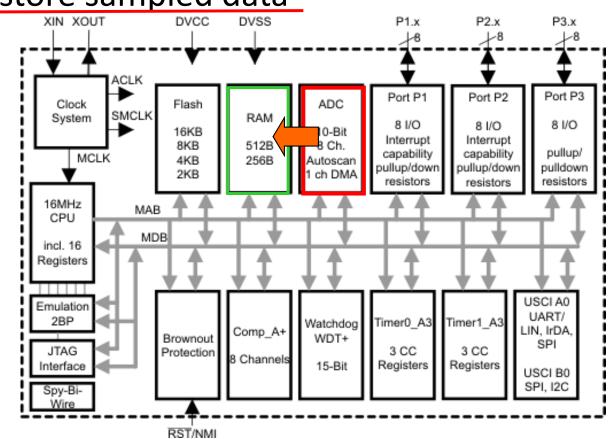




 Provide continuous sampling of multiple analog inputs and <u>store sampled data</u>

Use hardware (Data Transfer Controller, DTC) to move data from ADC to memory

Interrupt CPU when block transfer is completed



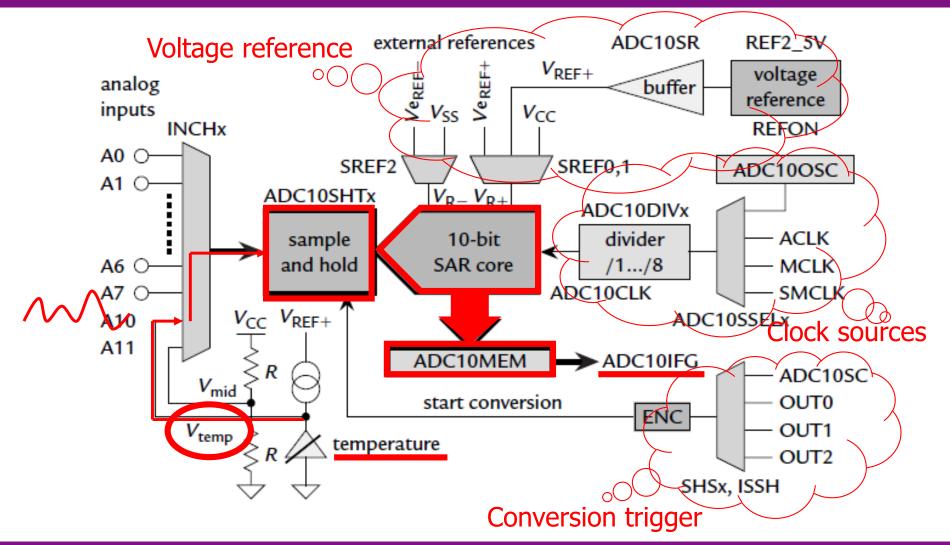


MSP430 may contain one or more converters:

- Comparator:
  - Compare the voltages on its two input terminals and return 0 or 1, e.g., Comparator\_A+
- Successive-approximation ADC:
  - Use binary search to determine the closest digital representation of the input signal, e.g. ADC10 and ADC12 to give 10 and 12 bits of output
- Sigma-delta ADC:
  - A more complicated ADC that gives higher resolution (more bits) but at a slower speed, e.g., SD16 and SD16\_A, both of which give a 16-bit output



## **Simplified Block Diagram of ADC10**

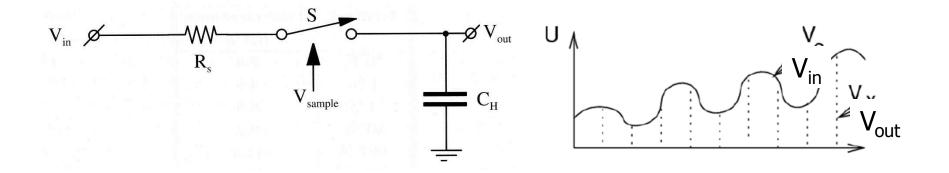




## Main Components of ADC10

• Sample-and-Hold circuit:

- V<sub>out</sub> = V<sub>in</sub> when V<sub>sample</sub> = 1

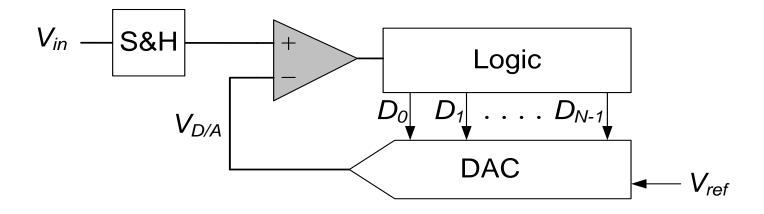


- SAR (Successive-Approximation Register):
  - 10-bit
  - Result written to ADC10MEM and raising ADC10IFG



#### **Successive-Approximation ADC**

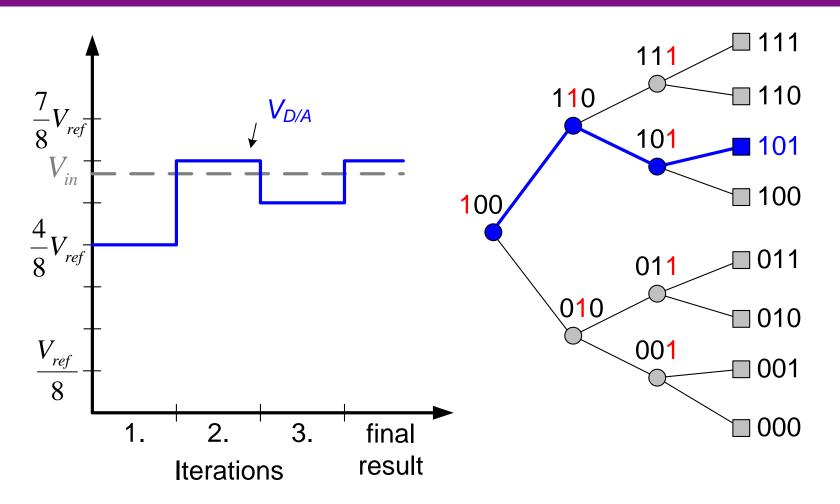
- Generate internal analog signal V<sub>D/A</sub> by DAC
- Compare V<sub>D/A</sub> with input signal V<sub>in</sub>
- Modify  $V_{D/A}$  by  $D_0 D_1 D_2 ... D_{N-1}$  until closest possible value to  $V_{in}$  is reached



Dr.-Ing. Frank Sill, Department of Electrical Engineering, Federal University of Minas Gerais, Brazil



#### **Successive-Approximation ADC**



P. Fischer, VLSI-Design - ADC und DAC, Uni Mannheim, 2005



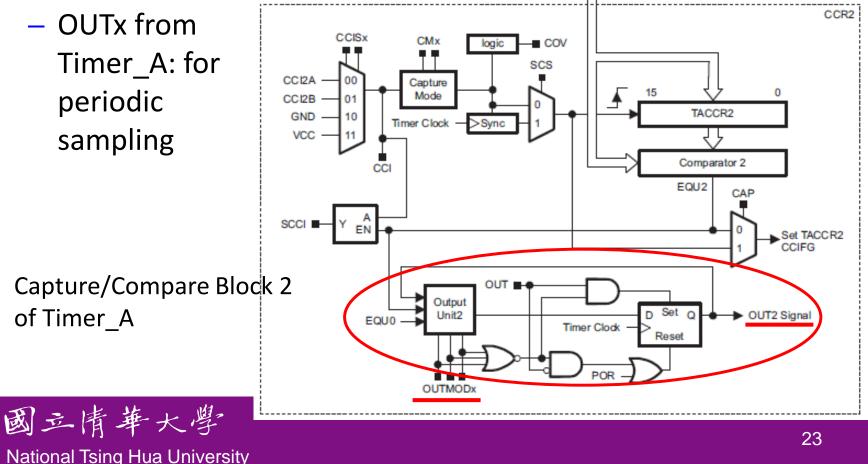
## Main Components of ADC10

- Built-in voltage reference:
  - Two selectable voltage levels, 2.5 V and 1.5 V
  - Setting REFON in ADC10CTL0 register to 1 enables the internal reference
  - Setting REF2\_5V in ADC10CTL0 to 1 selects 2.5 V as the internal reference, otherwise 1.5 V
  - After voltage reference is turned on, we must wait about
     30µs for it to settle



## Main Components of ADC10

- Sources of sample-and-hold circuit:
  - ADC10SC bit in ADC10CTL0 register, which can be set (and is thus triggered) by software, or



## Data Transfer Controller (DTC)

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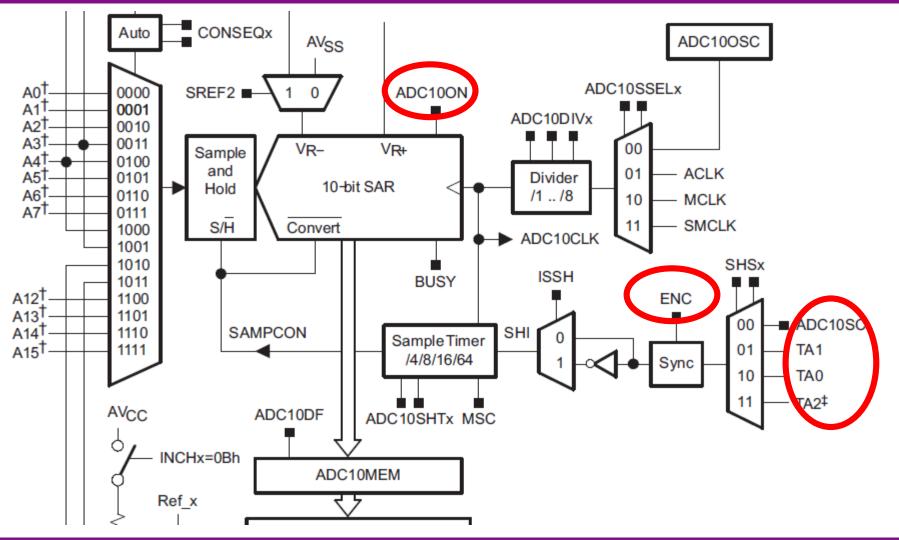
 Transfer conversion 1.5V or 2.5V or Reference results from ADC10MEM to Auto Avcc Avss other on-chip Input channel memory locations  $V_{R+}$  $V_{R_{-}}$ S/H 10-bit SAR Each load of ADC10MEM ADC10SC TA1 triggers a data TA0 ΤΑ2 **ADC10MEM** transfer until a set amount Batt Temp During each DTC RAM, Flash, Data Peripherals Transfer transfer, CPU is Controller halted 國立情華大學

## **ADC10** Interrupts

- One interrupt and one interrupt vector
  - When DTC is not used (ADC10DTC1 = 0), ADC10IFG is set when conversion results are loaded into ADC10MEM
  - When DTC is used (ADC10DTC1 > 0), ADC10IFG is set when a block transfer completes
- If both ADC10IE and GIE bits are set, then ADC10IFG generates an interrupt request
  - ADC10IFG is automatically reset when interrupt request is serviced, or it may be reset by software



## **Enabling Sampling and Conversion**





#### **Steps for Single Conversion**

(1) Configure ADC10, including the ADC100N bit to enable the module.

The ENC bit must be clear so that most bits in ADC10CTL0 and ADC10CTL1 can be changed.

(2) Set the ENC bit to enable a conversion.

This cannot be done while the module is being configured in the previous step.

(3) Trigger the conversion.

This is done either by setting the ADC10SC bit or by an edge from Timer\_A.

 ADC10ON, ENC, ADC10SC are all in control register ADC10CTL0

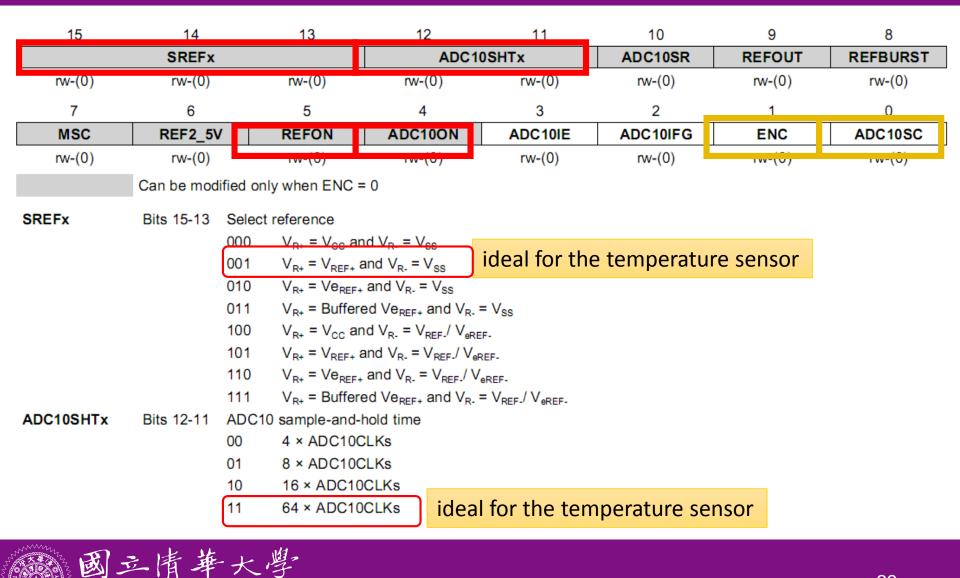


## **ADC10** Registers

Register	Short Form	Register Type	Addr.	Initial State
ADC10 input enable register 0	ADC10AE0	Read/write	04Ah	Reset with POR
ADC10 input enable register 1	ADC10AE1	Read/write	04Bh	Reset with POR
ADC10 control register 0	ADC10CTL0	Read/write	01B0h	Reset with POR
ADC10 control register 1	ADC10CTL1	OCTL1 Read/write		Reset with POR
ADC10 memory	ADC10MEM	Read	01B4h	Unchanged
register ()	here the a is saved	Read/write	048h	Reset with POR
ADC10 data transfer control register 1	ADC10DTC1	Read/write	049h	Reset with POR
ADC10 data transfer start address	ADC10SA	Read/write	01BCh	0200h with POR



## ADC10CTL0





### ADC10CTL0 cont'd

REFON	Bit 5	Reference generator on			
		0 Reference off			
		1 Reference on			
ADC10ON	Bit 4	ADC10 on			
		0 ADC10 off			
		1 ADC10 on			
ADC10IE	Bit 3	ADC10 interrupt enable			
		0 Interrupt disabled			
		1 Interrupt enabled			
ENC	Bit 1	Enable conversion			
		0 ADC10 disabled			
		1 ADC10 enabled			
ADC10SC	Bit 0	Start conversion. Software-controlled sample-and-conversion start. ADC10SC and ENC may be set together with one instruction. ADC10SC is reset automatically.			
		0 No sample-and-conversion start			
		1 Start sample-and-conversion			
ADC10CT	L0 = S	<pre>SREF_2 + ADC10SHT_1; // Reference range &amp; SH time</pre>			



#### ADC10CTL1

15	14	1	3	12	11	10	9	8
INCHx					SHSx		ADC10DF	ISSH
rw-(0)	rw-(0)	rw-	-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	ļ	5	4	3	2	1	0
	ADC10DIVx			ADC10	SSELx	CON	CONSEQx	
rw-(0)	rw-(0)	rw-	-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	r-0
	Can be mod	dified only whe	en ENC =	0				
INCHx	Bits 15-12	sequence of           0000         A0           0001         A1           0010         A2           0011         A3           0100         A4           0101         A5           0110         A6           0111         A7           1000         VeRE           1001         VeRE           1010         Ten           1011         (Vcc           1100         (Vcc           1101         (Vcc           1110         (Vcc	EF+ F-N <sub>eREF-</sub> nperature c - V <sub>SS</sub> ) / 2 c - V <sub>SS</sub> ) / 2	ons. sensor	0x22xx devices 0x22xx devices 0x22xx devices	a single-conversion	or the highest ch	annel for a
NNMM4 -		(•00		_,				



#### ADC10CTL1 cont'd

SHSx	Bits 11-10	Sample	e-and-hold source select	ct			
		00	ADC10SC bit	•			
		01	Timer_A.OUT1				
		10	Timer_A.OUT0				
		11	Timer_A.OUT2 (Time	er A.OUT1 on MSP43	30x20x2 devices	s)	
ADC10DF	Bit 9	ADC10	ADC10 data format				
		0	Straight binary				
		1	2s complement				
ISSH	Bit 8	Invert s	signal sample-and-hold	l			
		0	The sample-input sig	nal is not inverted.			
		1	The sample-input sig	nal is inverted.			
ADC10DIVx	Bits 7-5	ADC10 clock divider					
		000	/1	CONSEQx	Bits 2-1	Conve	ersion sequence mode select
		001	/2	CONCLAX	51672	00	Single-channel-single-conversion
		010	/3			01	
		011	/4				Sequence-of-channels
		100	/5			10	Repeat-single-channel
		101	/6			11	Repeat-sequence-of-channels
		110	/7				
		111	/8				
ADC10SSELx	Bits 4-3	ADC10 clock source select					
		00	ADC10OSC				
		01	ACLK				
		10	MCLK				
		11	SMCLK				

ADC10CTL1 = INCH\_10 + ADC10DIV\_0; // Temp Sensor ADC10CLK





- Introduction to analog-to-digital conversion
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- Repetitive single conversion:
  - A single sample is made on A1 with reference to Vcc
  - If A1 > 0.5\*Vcc, P1.0 set, else reset.
  - Software sets ADC10SC to start sample and conversion.
     ADC10SC automatically cleared at end of conversion.
  - Use ADC10 internal oscillator to time the sample and conversion.



```
#include "msp430.h"
void main(void) {
 WDTCTL = WDTPW + WDTHOLD; // Stop WDT
  // H&S time 16x, interrupt enabled
 ADC10CTL0 = ADC10SHT 2 + ADC10ON + ADC10IE;
 ADC10CTL1 = INCH 1; // Input A1
 ADC10AE0 |= 0 \times 02; // Enable pin A1 for analog in
  P1DIR |= 0 \times 01; // Set P1.0 to output
  for (;;) {
   ADC10CTL0 |= ENC + ADC10SC; // Start sampling
    bis SR register(CPUOFF + GIE); // Sleep
    if (ADC10MEM < 0x1FF) // 0x1FF = 511
      Plour \&= ~0x01; // Clear Pl.0 LED off
    else
     P1OUT = 0x01; // Set P1.0 LED on }
```



```
// ADC10 interrupt service routine
#pragma vector=ADC10 VECTOR
  interrupt void ADC10 ISR(void)
    bic SR register on exit(CPUOFF);
  // Clear CPUOFF bit from 0(SR)
}
```



- Continuous sampling driven by Timer\_A
  - A1 is sampled 16/second (ACLK/2048) with reference to 1.5V, where ACLK runs at 32 KHz driven by an external crystal.
  - If A1 > 0.5Vcc, P1.0 is set, else reset.
  - Timer\_A is run in up mode and its CCR1 is used to automatically trigger ADC10 conversion, while CCR0 defines the sampling period
  - Use internal oscillator times sample (16x) and conversion (13x).



```
#include "msp430.h"
void main(void) {
  WDTCTL = WDTPW + WDTHOLD; // Stop WDT
  // TA1 trigger sample start
 ADC10CTL1 = SHS 1 + CONSEQ 2 + INCH 1;
 ADC10CTL0 = SREF 1 + ADC10SHT 2 + REFON +
              ADC100N + ADC10IE;
  enable interrupt(); \gamma/ Enable interrupts.
  TACCR0 = 30; // Delay for Volt Ref to settle
  TACCTL0 |= CCIE; // Compare-mode interrupt.
  TACTL = TASSEL 2 + MC 1; // SMCLK, Up mode.
                          // Wait for settle.
  LPM0;
  TACCTLO \&= \sim CCIE;
                        // Disable timer Interrupt
   disable interrupt();
```



```
ADC10CTL0 |= ENC; // ADC10 Enable
ADC10AE0 |= 0 \times 02; // P1.1 ADC10 option select
P1DIR |= 0x01; // Set P1.0 output
TACCR0 = 2048-1; // Sampling period
TACCTL1 = OUTMOD 3; // TACCR1 set/reset
TACCR1 = 2046; // TACCR1 OUT1 on time
                          // ACLK, up mode
TACTL = TASSEL 1 + MC 1;
// Enter LPM3 w/ interrupt$
 bis SR register(LPM3 bits + GIE);
```

Timer\_A CCR1 out mode 3: The output (OUT1) is set when the timer *counts* to the TACCR1 value. It is reset when the timer *counts* to the TACCR0 value.



}

```
// ADC10 interrupt service routine
#pragma vector=ADC10 VECTOR
  interrupt void ADC10 ISR(void) {
  if (ADC10MEM < 0x155) // ADC10MEM = A1 > 0.5V?
    Plour \&= ~0x01; // Clear Pl.0 LED off
  else
    P1OUT |= 0 \times 01; // Set P1.0 LED on
}
#pragma vector=TIMERA0 VECTOR
  interrupt void ta0 isr(void) {
  TACTL = 0;
                        // Exit LPM0 on return
  LPMO EXIT;
```





- ADC: analog-to-digital conversion DAC: digital-to-analog conversion
  - Conversions will necessarily introduce errors. Important to understand constraints and limitations
- ADC10 in MSP430
  - Convert an analog signal into 10-bit digitals
  - Registers associated with ADC10
- Sample program of ADC10
  - Single conversion
  - Continuous conversion driven by Timer\_A

