

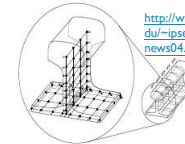
# Computer-aided design

## What is CAD?

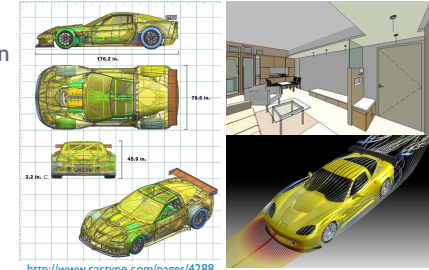
▶ Using computer technology for the process of design.

▶ Examples:

- ▶ Building interior-design
- ▶ Automotive
- ▶ High-speed train



<http://www4.ncsu.edu/~ipsen/ps/samnews04.pdf>

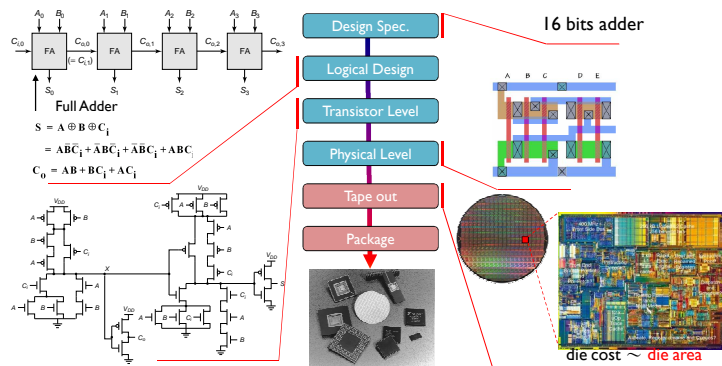


<http://www.cartype.com/pages/4288>

- ▶ Many more: aircraft, and aerospace industries, industrial and architectural design, ...
- ▶ We will focus on EDA(Electronic Design Automation)

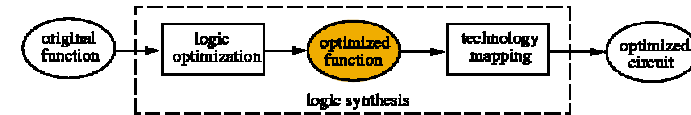
## EDA (Electronic Design Automation)

▶ IC design flow



▶ From Wai Kei Mak's lecture note

## Logical design/synthesis



▶ Optimization goals: minimize area, delay, power, etc

▶ Ex: Two-level: minimize the number of product terms.

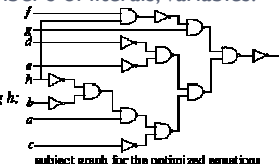
$$F = x_1x_2x_3 + x_1x_2x_3 + x_1x_2x_3 + x_1x_2x_3 + x_1x_2x_3 \Rightarrow F = x_2 + x_1x_3$$

▶ Ex: Multi-level: minimize the number's of literals, variables.

$$\begin{aligned} i1 &= a + b \quad c; \\ i2 &= d + e; \\ i3 &= a + b + c; \\ i4 &= i1 + i2 + f \quad g; \\ i5 &= i4 + h + i2 \quad i3; \\ F &= i5; \end{aligned}$$

logic optimization

$$\begin{aligned} i1 &= d + e; \\ i2 &= b + h; \\ i3 &= a + i2 + c; \\ i4 &= i1 + i3 + f \quad g \quad h; \end{aligned}$$



▶ 邏輯設計，離散數學，演算法

## Transistor-level design

- ▶ Switch-level simulation (treats transistors as switches)
- ▶ Circuit simulation or transistor-level simulation (most detailed analysis)

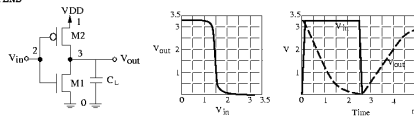
### ▶ Ex: Circuit Simulation of a CMOS Inverter (0.6 μm)

```
M1 3 2 0 0 nch W=1.2u L=0.6u AS=2.16p PS=4.8u AD=2.16p PD=4.8u
M2 3 2 1 1 pch W=1.8u L=0.6u AS=3.24p PS=5.4u AD=3.24p PD=5.4u
CL 3 0 0 0.2pF
```

```
VDD 1 0 3.3
VIN 2 0 DC 0 PULSE (0 3.3 0ns 100ps 100ps 2.4ns 5ns)
```

```
.LIB './mod.06' typical
```

```
.OPTION NOMOD POST INGOLD=2 NUMDGT=6 BRIEF
.DC VIN 0V 3.3V 0.001V
.PRINT DC V(3)
.TRAN 0.001N EN
.PRINT TRAN V(2) V(3)
.END
```



▶ 物理，電子電路，線性代數，演算法

## Physical (layout) design

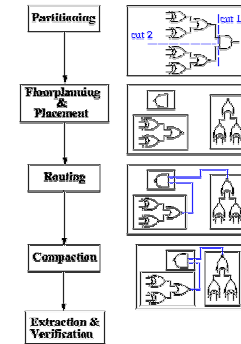
- ▶ Physical design converts a circuit description into a geometric description.

▶ The description is used to manufacture a chip.

### ▶ Physical design cycle:

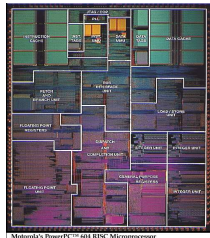
- ▶ Logic partitioning
- ▶ Floorplanning and placement
- ▶ Routing
- ▶ Compaction

- ▶ Others: circuit extraction, timing verification and design rule checking.

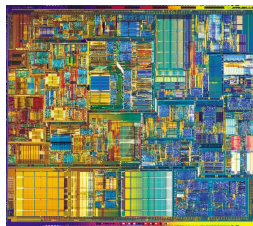


▶ 演算法，計算幾何演算法，最佳化

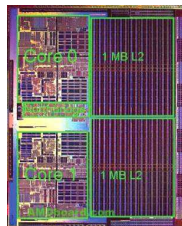
## Examples



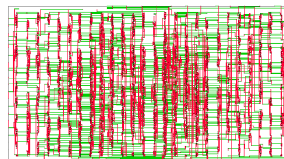
PowerPC 604 Floorplan



Pentium 4 Floorplan



AMD dual core



Routing Example  
0.18um technology,  
pitch = 1 um, 2774 nets.

▶